PCI Express Architecture PHY Test Specification

Revision 4.0, Version 0.9

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Revision History

Revision	Version	History	Date
4.0	0.9	• Miscellaneous updates • Added Appendix D • Added Spread Sheet for Fixture Calibration • Added Vswing • Added Appendix D, Alternate Method of System TX Signal Quality Test at 16GT/s	April 23, 2019

Contact the PCI-SIG office to obtain the latest revision of this specification.

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1. Introduction

This document provides test descriptions for PCI Express electrical testing. It is relevant for anyone building Add-in Cards or system boards to the PCI Express Card Electromechanical Specification 4.0. This specification does not describe the full set of PCI Express tests and assertions for these devices.

Devices must also meet the requirements and tests described in the latest versions of the following documents as well as any other tests provided by the PCI-SIG:

- *PCI Express Architecture Configuration Space Test Specification*
- *Platform BIOS Test Considerations for the PCI Express Architecture*
- *PCI Express Architecture Link Layer Test Specification*
- *PCI Express Architecture Transaction Layer Test Specification*
- *PCI Express Retimer Test Specification*

1.1 Coverage

This document covers items in the PCI Express Card Electromechanical Revision 4.0 or Base Specification Revision 4.0 that apply to 16 GT/s, 8.0 GT/s, 5.0 GT/s and 2.5 GT/s signaling. 5.0 GT/s signaling requirements described in the PHY Electrical Test Consideration Revision 2.0 document apply to PCIe 2.0 devices that support 5.0GT/s and 2.5 GT/s signaling. 2.5 GT/s signaling requirements described in the PHY Electrical Test Considerations Revision 1.1 document apply to PCIe2.0, PCIe 1.1 and PCIe 1.0a devices that support 2.5 GT/s signaling.

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2. Test Descriptions

2.1 Add-in Card Transmitter Signal Quality

This test is run on all card electromechanical (CEM) form factor add-in cards. The test verifies that the signaling of the system at 2.5 GT/s, 5.0 GT/s, 8.0 GT/s and 16.0 GT/s with a specified transmitter equalization values meets eye diagram and other jitter requirements.

2.1.1 Starting Configuration

This test is run with devices in the polling.compliance state. This state must be supported to run the test.

2.1.2 Overview of Test Steps

The test is performed by following these steps:

1. Insert the Add-in Card under test into a compliance base board (CBB) without power. A CBB revision 4.0 must be used at all data rates if 16 GT/s is supported. If the maximum supported data rate is 2.5 GT/s, 5.0 GT/s or 8.0 GT/s, a CBB revision 3.0 may be used for this test.
2. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the CBB main board are connected to receive lane zero (SMP connectors J18 and J2) on the CBB riser card via appropriate SMP to SMP cables.
3. Terminate all Tx lanes with 50-ohm terminations except the lane under test.
4. Connect the Tx lane under test to a high-speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
5. Power on the CBB.
6. Push the compliance toggle button on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the Add-in Card under test) until the compliance mode is 2.5 GT/s.
7. Perform electrical compliance test for 2.5 GT/s.

8. Push the compliance toggle button on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the Add-in Card under test) until the compliance mode is 5.0 GT/s with 3.5 dB de-emphasis.
9. Perform electrical compliance test for 5.0 GT/s and 3.5 dB de-emphasis.
10. Push the compliance toggle button on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the Add-in Card under test) until the compliance mode is 5.0 GT/s with 6.0 dB de-emphasis.
11. Perform electrical compliance test for 5.0 GT/s and 6.0 dB de-emphasis.
12. Perform electrical compliance test for 8.0 GT/s (see section 2.1.4).
13. Perform electrical compliance test for 16.0 GT/s (see section 2.1.5). Power down the CBB and remove the add-in card.

2.1.3 Add-in Card Transmitter Electrical Compliance Test for 2.5 GT/s and 5.0 GT/s

1. Measure the transmitted waveform with a high-speed oscilloscope or equivalent data capture instrument.
2. Capture one (1) million unit -intervals of data at 5.0 GT/s and 250,000 intervals of data at 2.5 GT/s. (250,000 X 400.0ps = 100.0µs at 2.5 GT/s, 10^6 X 200.0ps = 200.0µs at 5.0 GT/s).
3. Measure eye amplitude and eye width using the SigTest analysis program with the appropriate (2.5 or 5.0 GT/s) Add-in Card template file.
4. The SigTest analysis program will also indicate if the acquired data pattern matches the expected compliance pattern. (this check is informative)
5. The test operator should confirm that the test pattern is a compliance pattern. If the pattern is a link training sequence or a clock pattern the device fails.
6. If the SigTest analysis program indicates that the Add-in Card passes, the electrical compliance test is complete.
7. Repeat the test for each lane.

2.1.4 Add-in Card Transmitter Electrical Compliance Test for 8.0 GT/s

1. Push the compliance toggle button (if the correct Transmitter Equalization setting is known) on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the Add-in Card under test) until the correct Tx EQ is selected, otherwise, push the compliance toggle button until the initial 8 GT/s Tx EQ preset is selected.
2. Measure the transmitted waveform with a high-speed oscilloscope or equivalent data capture instrument.
3. Capture 1.6 million unit-intervals of data (1.6 X 10^6 X 125.0ps = 200.0µs).

> **Note:** The portion of the 8.0 GT/s Add-in Card Test Channel not present on the CBB will be embedded into the captured waveform by the Sigtest. The s-parameters to be embedded are included with this specification.

4. Measure eye amplitude and eye width using SigTest analysis program with the 8 GT/s Add-in Card test template file (eye height 50 mV and eye width 45 ps).

> **Note:** These limits are more constrained than the limits in the PCI Express Card Electromechanical (CEM) specification to account for the clean clock in the CBB fixture.

5. The SigTest analysis program will also indicate if the acquired data pattern matches the expected compliance pattern (this check is informative).
6. If the SigTest analysis program indicates that the Add-in Card passes, the electrical compliance test is complete. If SigTest indicates the Add-in Card fails, the next Tx EQ setting should be selected (by pushing the compliance toggle button) and steps 2 through 6 of this test procedure should be repeated until the Add-in Card passes or all Tx EQ settings have been tested.
7. Repeat the test for each lane.

2.1.5 Add-in Card Transmitter Electrical Compliance Test for 16.0 GT/s

1. Connect the Tx lane under test on the CBB to the differential pair of the Variable ISI board which provides a physical channel insertion loss of 15dB at 8 GHz (See Appendix C). Connect the output of the Variable ISI board to a high-speed oscilloscope or equivalent data capture instrument via low loss SMA cables.
2. If the correct Transmitter Equalization setting is known push the compliance toggle button on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the Add-in Card under test) until the correct Tx EQ is selected, otherwise, push the compliance toggle button until the initial 16 GT/s Tx EQ preset is selected.
3. Measure the transmitted waveform with a high-speed oscilloscope or equivalent data capture instrument with the maximum bandwidth set to 25GHz.
4. Capture 2.0 million unit-intervals of data ($2.0 \times 10^6 \times 62.5$ps = 125.0 µs).

> **Note:** The Root Complex package is embedded into the captured waveform on the scope or by Sigtest. The s-parameters to be embedded are included with this specification.

5. Measure Extrapolated Eye Height and Minimum Eye Width using the SigTest analysis program with the 16 GT/s Add-in Card test template file (PCIE_4_0_CARD\PCIe_4_16G_CEM.dat).
6. The SigTest analysis program will also indicate if the acquired data pattern matches the expected compliance pattern. (this check is informative)
7. If the SigTest analysis program indicates the Add-in Card Minimum Eye Width is greater than or equal to 24.75 ps and Extrapolated Eye height is greater than or equal to 23 mV, the electrical compliance test passes and is complete. If SigTest indicates the Add-in Card fails, the next Tx EQ setting should be selected (by pushing the compliance toggle button) and steps 2 through 6 of this test procedure should be repeated until the Add-in Card passes or all Tx EQ settings have been tested.

> **Note:** These limits are less constrained than the limits in the PCI Express Card Electromechanical (CEM) specification to account for the clean clock in the CBB and less far end crosstalk on the test fixture channel.

8. Repeat the test for each lane.

> **Note:** An alternate mechanism may be used to get to the appropriate TX compliance state.

2.2 Add-in Card Transmitter Pulse Width Jitter Test at 16 GT/s

This test is run on all card electromechanical form factor Add-in Cards that operate at 16.0 GT/s. This test verifies that the Add-in Card produces a Pulse Width Jitter (PWj) below the *PCIe Base Specification* limit.

2.2.1 Starting Configuration

This test is run with devices in the polling.compliance state. This state must be supported to run the test.

2.2.2 Overview of Test Steps

The test is performed by following these steps:

1. Insert the Add-in Card under test into a compliance base board (CBB) revision 4.0 without power.
2. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the CBB main board are connected to receive lane zero (SMP connectors J18 and J2) on the CBB riser card via appropriate SMP to SMP cables.
3. Terminate all Tx lanes with 50-ohm terminations except for Lane 0.
4. Connect the Tx lane under test to a high-speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
5. Power on the CBB.
6. Push the compliance toggle button on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the Add-in Card under test) until the pattern is the 16.0 GT/s Jitter Measurement Pattern (Lanes 0/8/16/24—setting #27 in the 4.0 *PCIe Base Specification*.).
7. Measure the transmitted waveform with a high-speed oscilloscope or equivalent data capture instrument with the maximum bandwidth set to 25 GHz.
8. Capture 2.0 million unit-intervals of data (2.0 X 10^6 X 62.5ps = 125.0 µs).

> **Note:** The Non-Root Complex package will not be embedded into the captured waveform on the scope or by Sigtest.

9. Measure Uncorrelated PWJ Tj @ E-12 using the SigTest analysis program with the 16 GT/s Pulse Width Jitter template file (PCIE_4_0_CARD\ PCIe_4_16GB_Tx_PWJ.dat).

10. If the SigTest analysis program indicates the Add-in Cards Uncorrelated PWJ Tj @ E-12 is less than or equal to 12.5 ps the electrical compliance test passes and is complete for this lane.

> **Note:** An alternate mechanism may be used to get to the appropriate TX compliance state.

2.3 Add-in Card Transmitter Preset Test

This test is run on all card electromechanical form factor Add-in Cards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the Add-in Card produces the correct transmitter equalization values for each preset in the set of 11 presets.

2.3.1 Starting Configuration

This test is run with devices in the polling.compliance state. This state must be supported to run the test.

2.3.2 Add-in Card Transmitter Preset Test for 8.0 GT/s

1. Insert the Add-in Card under test into a CBB revision 3.0 or 4.0 without power.
2. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the CBB main board are connected to receive lane zero (SMP connectors J18 and J2) on the CBB riser card via appropriate SMP to SMP cables.
3. Terminate all Tx Lanes with 50-ohm terminations except the lane under test.
4. Connect the Tx lane under test to a high-speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
5. Power on the CBB
6. Set Add-in Card to the initial 8.0 GT/s test state using the compliance toggle button on the CBB.

> **Note:** An alternate mechanism may be used to get to the appropriate TX compliance state.

7. Capture 1.6 million unit-intervals of data ($1.6 \times 10^6 \times 125.0\text{ps} = 200.0\mu\text{s}$). Save the captured waveform to a file with a unique name to identify which preset was enabled when the waveform was captured. The captured data pattern should be compliance pattern and must contain runs of 64 ones and 64 zeros.
8. Press the compliance toggle button to cause the card under test to change to the next transmitter equalization preset value.

9. Repeat steps seven and eight until all 11 presets have been captured and saved.

> **Note:** The waveforms from test 2.1.2 can be used allowing steps one through nine to be skipped.

10. Use the SigTest Transmitter Preset Test option to read the saved waveform files and compute the preset values from these. All preset values must be within their specified limits.

2.3.3 Add-in Card Transmitter Preset Test for 16.0 GT/ s

1. Insert the Add-in Card under test into a CBB revision 3.0 or 4.0 without power.

> **Note:** The Variable ISI board from the revision 4.0 test fixtures must not be used for this test.

2. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the CBB main board are connected to receive lane zero (SMP connectors J18 and J2) on the CBB riser card via appropriate SMP to SMP cables.
3. Terminate all Tx lanes with 50-ohm terminations except the lane under test.
4. Connect the Tx lane under test to a high-speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
5. Power on the CBB
6. Set Add-in Card to the initial 16.0 GT/s test state using the compliance toggle button on the CBB.

> **Note:** An alternate mechanism may be used to get to the appropriate TX compliance state.

7. Capture 2.0 million unit-intervals of data ($2.0 \times 10^6 \times 62.5ps = 125.0\mu s$). Save the captured waveform to a file with a unique name to identify which preset was enabled when the waveform was captured. The captured data pattern should be compliance pattern and must contain runs of 64 ones and 64 zeros.
8. Press the compliance toggle button to cause the card under test to change to the next transmitter equalization preset value.
9. Repeat steps seven and eight until all 11 presets have been captured and saved.
10. Use the SigTest Transmitter Preset Test option to read the saved waveform files and compute the preset values from these. All preset values must be within their specified limits.

2.4 Add-in Card Transmitter Initial TX EQ Test

This test is run on all card electromechanical form factor Add-in Cards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the Add-in Card will start with the correct TX EQ preset requested through the protocol.

2.4.1 Starting Configuration

A protocol aware signal source and receiver such as a Protocol Test Card (PTC), Bit Error Ratio Tester (BERT), other specialized test equipment or any combination of different test equipment that can perform the test is connected to the device under test via a CBB. Since it is necessary to send commands to the DUT to adjust the transmitter equalization values and to get the DUT into loopback mode in order to perform this test, the test equipment must be able to perform the sequence of steps outlined in the *PCI Express Base Specification*, Rev. 4.0, sections 4.2.6.4.2 and in this document's Appendix A: Getting into Loopback for 8GT/s & 16GT/s.

2.4.2 Add-in Card Transmitter Initial TX EQ test for 8.0 GT/s

1. Insert the Add-in Card under test into a CBB revision 3.0 or 4.0 without power.
2. Connect the transmitter output of the protocol aware test equipment to the Rx SMP connectors on the CBB lane under test via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
3. Connect the 100 MHz reference clock output from the test equipment to the clock input SMP connectors on the CBB.
4. Tx lanes other than the lane under test should be unterminated.
5. Connect the Tx lane under test to signal splitters with one set of outputs going to the receiver inputs of the protocol aware test equipment and the other set of outputs going to a high-speed oscilloscope or equivalent data capture instrument. All connections to the CBB should be made via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables. All other connections should be made via phase matched, low loss SMA cables.
6. Power on the CBB.
7. Have the test equipment train the DUT and negotiate to 8.0 GT/s requesting P0 as the initial preset for the DUT. The test equipment does not request any TX EQ adjustments in phase 3.
8. Verify that the TX EQ preset for the DUT stays consistent once it transitions to 8 GT/s.
9. Have the test equipment put the DUT into loopback and transmit the compliance pattern so that it gets returned to the test equipment and oscilloscope.
10. Capture 1.6 million unit-intervals of data ($1.6 \times 10^6 \times 125.0$ps = 200.0µs). Save the captured waveform to a file with a unique name to identify that this waveform is for preset P0.

11. Repeat the test for the equivalent of each preset from P0 to P9.
12. Use the SigTest Transmitter Preset Test option to read the saved waveform files and compute the preset values from these. All preset values must be within their specified limits.

2.4.3 Add-in Card Transmitter Initial TX EQ test for 16.0 GT/s

1. Insert the Add-in Card under test into a CBB revision 4.0 without power.
2. Connect the transmitter output of the protocol aware test equipment to the Rx SMP connectors on the CBB lane under test via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
3. Connect the 100 MHz reference clock output from the test equipment to the clock input SMP connectors on the CBB.
4. Tx lanes other than the lane under test should be unterminated.
5. Connect the Tx lane under test to signal splitters with one set of outputs going to the receiver inputs of the protocol aware test equipment and the other set of outputs going to a high-speed oscilloscope or equivalent data capture instrument. All connections to the CBB should be made via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables. All other connections should be made via phase matched, low loss SMA cables.
6. Power on the CBB.
7. Have the test equipment train the DUT and negotiate to 16.0 GT/s requesting P0 as the initial preset for the DUT. The test equipment does not request any TX EQ adjustments in phase 3.
8. Verify that the TX EQ preset for the DUT stays consistent once it transitions to 16 GT/s.
9. Have the test equipment put the DUT into loopback and transmit the compliance pattern so that it gets returned to the test equipment and oscilloscope.
10. Capture 2.0 million unit-intervals of data ($2.0 \times 10^6 \times 62.5$ps = 125.00µs). Save the captured waveform to a file with a unique name to identify that this waveform is for preset P0.
11. Repeat the test for the equivalent of each preset from P0 to P9.
12. Use the SigTest Transmitter Preset Test option to read the saved waveform files and compute the preset values from these. All preset values must be within their specified limits.

2.5 Add-in Card Transmitter Link Equalization Response Test

This test is run on all card electromechanical form factor Add-in Cards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the Add-in Card will respond correctly to transmitter equalization commands sent via the link protocol.

2.5.1 Starting Configuration

A protocol aware signal source and receiver such as a Protocol Test Card (PTC), Bit Error Ratio Tester (BERT), other specialized test equipment or any combination of different test equipment is connected to the device under test via a CBB. Since it is necessary to send commands to the DUT to adjust the transmitter equalization values and to get the DUT into loopback mode in order to perform this test, the test equipment must be able to perform the sequence of steps outlined in the *PCI Express Base Specification*, Rev. 4.0, sections 4.2.6.4.2 and in this document's Appendix A: Getting into Loopback.

2.5.2 Add-in Card Transmitter Link Equalization Response Test for 8.0 GT/s

1. Insert the Add-in Card under test into a CBB revision 3.0 or 4.0 without power.
2. Connect the transmitter output of the protocol aware test equipment to the Rx SMP connectors on the CBB lane under test via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
3. Connect the 100 MHz reference clock output from the test equipment to the clock input SMP connectors on the CBB.
4. Tx lanes other than the lane under test can be terminated with 50-ohm terminations or unterminated – as requested by the device under test provider.
5. Connect the Tx lane under test to signal splitters with one set of outputs going to the receiver inputs of the protocol aware test equipment and the other set of outputs going to a high-speed oscilloscope or equivalent data capture instrument (if the protocol aware test equipment is capable of acquiring the signal on its receiver and saving it to a file, the splitters and oscilloscope can be omitted). All connections to the CBB should be made via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables. All other connections should be made via phase matched, low loss SMA cables.
6. Power on the CBB.
7. Have the test equipment train the DUT and negotiate to 8.0 GT/s.
8. Have the test equipment send a command to the DUT to set its transmitter equalization to preset 4.
9. Verify that the requested equalization change is complete within 1 microsecond from when the test equipment first sends the request. Note – the test equipment operator must be able to determine when the first request was sent relative to the observed TX EQ changed in the DUT. The test equipment/operator records the cursors reported by the device under test for the preset being tested.
10. Have the test equipment put the DUT into loopback and transmit the compliance pattern so that it gets returned to the test equipment and oscilloscope.

11. Capture 1.6 million unit-intervals of data (1.6 X 10^6 X 125.0ps = 200.0µs). Save the captured waveform to a file with a unique name to identify that this waveform mimics preset four.
12. Repeat steps 6-11 for each preset from P0 to P9.
13. Use the SigTest Transmitter Preset Test option to read the ten saved waveform files and compute the preset values from these. All preset values computed must be within their specified limits.
14. The test is repeated with each request for the device under test TX equalization using the cursors reported by the device under test for that preset.

2.5.3 Add-in Card Transmitter Link Equalization Response Test for 16.0 GT/s

Note: The initial preset sent by the AIC must be different than the preset requested by the test equipment used for measuring the response time. The initial preset also must be different enough electrically as to allow a noticeable change to the voltage level on the scope.

1. Insert the Add-in Card under test into a CBB revision 4.0 without power.
2. Connect the transmitter output of the protocol aware test equipment to the Rx SMP connectors on the CBB lane under test via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
3. Connect the 100 MHz reference clock output from the test equipment to the clock input SMP connectors on the CBB.
4. Tx lanes other than the lane under test can be terminated with 50-ohm terminations or unterminated – as requested by the device under test provider.
5. Connect the Tx lane under test to signal splitters with one set of outputs going to the receiver inputs of the protocol aware test equipment and the other set of outputs going to a high-speed oscilloscope. All connections to the CBB should be made via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables. All other connections should be made via phase matched, low loss SMA cables.

   Note: The Variable ISI board is not used for this test.

6. Power on the CBB
7. Have the test equipment train the DUT and negotiate to 16.0 GT/s with an initial preset other than the Preset set in step 8.
8. Have the test equipment send a command to the DUT to set its transmitter equalization to preset 0.

9. Verify that the requested equalization change is complete within 1 microsecond from when the test equipment first sends the request. Note – the test equipment operator must be able to determine when the first request was sent relative to the observed TX EQ changed in the DUT. The test equipment/operator records the cursors reported by the device under test for the preset being tested.
10. Have the test equipment put the DUT into loopback and transmit the compliance pattern so that it gets returned to the test equipment and oscilloscope.
11. Capture 2.0 million unit-intervals of data ($2.0 \text{ X } 10^6 \text{ X } 62.5\text{ps} = 125.0\mu\text{s}$). Save the captured waveform to a file with a unique name to identify that this waveform mimics preset four.
12. Repeat steps 6-11 for each preset from P1 to P9.
13. Use the SigTest Transmitter Preset Test option to read the ten saved waveform files and compute the preset values from these. All preset values computed must be within their specified limits.
14. The test is repeated with each request for the device under test TX equalization using the cursors reported by the device under test for that preset.

2.6 Add-in Card Lane Margining at 16 GT/s

The Add-in Card LMT tests whether the Add-in Card under test implements the lane margining capability but the margin value reported is not checked against any traceable metric. This test is run on all card electromechanical form factor Add-in Cards that operate at 16.0 GT/s. This test checks the on-die lane margining of an Add-in Card receiver using a Gold system by adjusting the Transmitter signal quality (e.g. TX Preset, TX Jitter, Vswing, Channel Loss) and looking for a change in the timing margin and voltage margin (optional). If there is at least one Retimer present on the Add-in Card under test, the lane margin test shall only be performed on the Retimer's receiver facing the edge fingers. This case requires knowledge of the Retimer's presence so the test equipment or the Lane Margin Tool can be configured to communicate to the indicated receiver using the appropriate protocol.

1. Insert the Add-in Card under test into a 16 GT/s capable Gold system.
2. Power on the Gold system.
3. Allow the Gold system to train the Add-in Card under test into L0 at 16 GT/s.
4. Use the Gold system to change the TX signal sent to the AIC receiver under test. System TX parameters such as TX Preset, TX jitter, Vswing, Channel loss can be adjusted for this purpose on the system TX.
5. Use the system software or Lane Margining Tool installed on the Gold system to send margin commands to the Add-in Card under test receiver or Retimer receiver, if applicable. Report and record the timing and, if applicable, voltage margins.
6. Repeat steps 3 through 5 by changing one of the system TX parameters listed in Step-4 and record timing and if applicable, Voltage values.

7. If a noticeable change to the timing margin is observed between steps 5 and 6, the test is passed. If voltage margining is supported, a change should also be observed but is not required.
8. This test is performed on Lane 0.

2.7 System Board Transmitter Signal Quality

This test is run on all card electromechanical form factor system boards. The test verifies that the signaling of the system at 2.5 GT/s, 5.0 GT/s, 8.0 GT/s and 16.0 GT/s with a specified transmitter equalization values meets eye diagram and other jitter requirements.

2.7.1 Starting Configuration

This test is run with devices in the polling.compliance state. This state must be supported to run the test.

2.7.2 Overview of Test Steps

The test performed by following these steps:

1. Power down the system under test.
2. Insert the compliance load board (CLB) into the slot for test. A CLB revision 4.0 must be used at all data rates if 16 GT/s is supported. If the maximum supported data rate is 2.5 GT/s, 5.0 GT/s or 8.0 GT/s, a CLB revision 3.0 may be used for this test.
3. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the front of the CLB are connected to receive lane zero (SMP connectors JXX and JX) on the back of the CLB via appropriate SMP to SMP cables.
4. Terminate all lanes with 50-ohm terminations except the lane under test.
5. Connect the lane under test to a high-speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
6. Connect the clock signal to the high-speed oscilloscope or equivalent data capture instrument via the reference clock SMP connectors on the CLB. The clock must have SSC enabled or disabled to be consistent with settings for the system during normal operation.
7. Power on the system under test.
8. Set the system to initial test state (e. g. 2.5 GT/s, -3.5dB de-emphasis).
9. Perform electrical compliance test for 2.5 GT/s and 5.0 GT/s (see section 2.8.1).
10. If the system supports the 8.0 GT/s data rate, perform electrical compliance test for 8.0 GT/s (see section 2.8.2).

11. If the system supports the 16.0 GT/s data rate, perform electrical compliance test for 16 GT/s (see section 2.8.3).
12. Power down the system and remove the CLB.

2.7.3 System Board Transmitter Electrical Compliance Test for 2.5 GT/s and 5.0 GT/s

1. Measure transmitted clock and data waveforms simultaneously with a high-speed oscilloscope or equivalent data capture instrument.
2. Capture 1 million unit-intervals of data and clock (10^6 X 400.0ps = 400.0µs at 2.5 GT/s, 10^6 X 200.0ps = 200.0µs at 5.0 GT/s).
3. Measure eye amplitude and eye width using the SigTest analysis program with the appropriate choice of template file. Template files differ based on data rate, transmitter equalization (de-emphasis) settings and the type of device under test (Add-in Card or system).
4. The SigTest analysis program will also indicate if the acquired data pattern matches the expected compliance pattern. (this check is informative)
5. The test operator should confirm that the test pattern is a compliance pattern. If the pattern is a link training sequence or a clock pattern the device fails.
6. Push the compliance toggle button on the CLB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the Add-in Card under test) until the compliance mode is either 5.0 GT/s and 3.5 dB or 5.0 GT/s and 6.0 dB – whichever will be used by the system in real operation...
7. Repeat steps 1-5.
8. Repeat the test for each lane.

Note: An alternate mechanism may be used to get to the appropriate TX compliance state.

2.7.4 System Board Transmitter Electrical Compliance Test for 8.0 GT/s

1. If the correct Transmitter Equalization setting is known, push the compliance toggle button on the CLB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the motherboard under test) until the correct Tx EQ is selected, otherwise push the compliance toggle button until the initial 8 GT/s Tx EQ preset is selected.
2. Measure transmitted clock and data waveforms simultaneously with a high-speed oscilloscope or equivalent data capture instrument.
3. Confirm that the waveform is the correct compliance pattern.

4. Capture 1.6 million unit-intervals of data (1.6 X 10^6 X 125.0ps = 200.0µs).

> **Note:** The portion of the 8.0 GT/s System Board Test Channel not present on the CLB will be embedded into the captured data waveform by Sigtest. The s-parameters to be embedded are included with this specification.

5. Measure eye amplitude and eye width using SigTest analysis program with the appropriate choice of template file. Template files differ based on data rate, transmitter equalization settings and the type of device under test (Add-in Card or system).
6. The SigTest analysis program will also indicate if the acquired data pattern matches the expected compliance pattern. (this check is informative)
7. If the SigTest analysis program indicates that the system board passes, the, electrical compliance test is complete. If SigTest indicates the system board fails, push the compliance toggle button on the CLB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the motherboard under test) to select the next Tx EQ setting and steps 2 through 7 of this test procedure should be repeated until the system board passes or all Tx EQ settings have been tested.
8. Repeat the test for each lane.

> **Note:** An alternate mechanism may be used to get to the appropriate TX compliance state.

2.7.5 System Board Transmitter Electrical Compliance Test for 16.0 GT/s

1. Connect the Tx lane under test on the CLB to the differential pair of the Variable ISI board which provides a physical channel insertion loss of 5dB at 8 GHz (See Appendix C). Connect the output of the Variable ISI board to a high-speed oscilloscope or equivalent data capture instrument via low loss SMA cables.
2. Connect the Reference Clock (REF CLK) on the CLB to a high-speed oscilloscope or equivalent data capture instrument via low loss SMA cables.
3. If the correct Transmitter Equalization setting is known, push the compliance toggle button on the CLB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the motherboard under test) until the correct Tx EQ is selected, otherwise push the compliance toggle button until the initial 16 GT/s Tx EQ preset is selected.
4. Measure transmitted clock and data waveforms simultaneously with a high-speed oscilloscope or equivalent data capture instrument with the maximum bandwidth set to 25GHz
5. Confirm that the waveform is the correct compliance pattern.

6. Capture 2.0 million unit-intervals of data and clock (2.0 X 10^6 X 62.5ps = 125.0µs) simultaneously.

> **Note:** The Non-Root Complex package model will be embedded into the captured data waveform on the scope or by Sigtest. The s-parameters to be embedded are included with this specification.

7. Measure Extrapolated Eye Height and Minimum Eye Width using SigTest analysis program with the appropriate choice of template file (PCIE_4_0_SYS\ PCIE_4_16GB_CEM_DUAL_PORT.dat).
8. The SigTest analysis program will also indicate if the acquired data pattern matches the expected compliance pattern. (this check is informative)
9. If the SigTest analysis program indicates the system board Minimum Eye Width is greater than or equal to 21.75ps and Extrapolated Eye Height is greater than or equal to 19mV, the, electrical compliance test passes and is complete. If SigTest indicates the system board fails, the next Tx EQ setting should be selected (by pushing the compliance toggle button) and steps 3 through 8 of this test procedure should be repeated until the system board passes or all Tx EQ settings have been tested.
10. Repeat the test for each lane.

> **Note:** An alternate mechanism may be used to get to the appropriate TX compliance state.

2.8 System Board Transmitter Preset Test

This test is run on all card electromechanical form factor system boards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the system board produces the correct transmitter equalization values for each preset in the set of 11 presets.

2.8.1 Starting Configuration

This test is run with devices in the polling.compliance state. This state must be supported to run the test.

2.8.2 System Board Transmitter Preset Test for 8.0 GT/s

The test is performed by following these steps:

1. Power down the system under test.
2. Insert the compliance load board revision 3.0 or 4.0 into the slot to be tested.
3. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the front of the CLB are connected to receive lane zero (SMP connectors JXX and JX) on the back of the CLB via appropriate SMP to SMP cables.
4. Connect the Tx lane under test to a high-speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
5. Power on the system under test.
6. Set system to the initial 8.0 GT/s test state using the compliance toggle button on the CLB.
7. Capture 1.6 million unit-intervals of data (1.6 X 10^6 X 125.0ps = 200.0µs). Save the captured waveform to a file with a unique name to identify which preset was enabled when the waveform was captured. The captured data pattern should be compliance pattern and must contain runs of 64 ones and 64 zeros. Press the compliance toggle button to cause the system under test to change to the next transmitter equalization preset value.
8. Repeat steps seven and eight until all 11 presets have been captured and saved.

> **Note:** The waveforms from Test 2.8.2 and 2.8.3 can be used allowing steps one through nine to be skipped.

9. Power down the system and remove the CLB.
10. Use the SigTest Transmitter Preset Test option to read the saved waveform files and compute the preset values from these. All preset values must be within their specified limits.

2.8.3 System Board Transmitter Preset Test for 16.0 GT/s

1. The test is performed by following these steps:
2. Power down the system under test.
3. Insert the compliance load board revision 3.0 or 4.0 into the slot to be tested.
4. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the front of the CLB are connected to receive lane zero (SMP connectors JXX and JX) on the back of the CLB via appropriate SMP to SMP cables.
5. Connect the Tx lane under test to a high-speed oscilloscope or equivalent data capture instrument via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
6. Power on the system under test.

7. Set system to the initial 16.0 GT/s test state using the compliance toggle button on the CLB.
8. Capture 1.6 million unit-intervals of data (1.6 X 10^6 X 62.5ps = 100.0µs). Save the captured waveform to a file with a unique name to identify which preset was enabled when the waveform was captured. The captured data pattern should be compliance pattern and must contain runs of 64 ones and 64 zeros. Press the compliance toggle button to cause the system under test to change to the next transmitter equalization preset value.
9. Repeat step seven until all 11 presets have been captured and saved.
10. Power down the system and remove the CLB.
11. Use the SigTest Transmitter Preset Test option to read the saved waveform files and compute the preset values from these. All preset values must be within their specified limits.

2.9 System Board Transmitter Link Equalization Response Test

This test is run on all card electromechanical form factor system boards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the system will respond correctly to transmitter equalization commands sent via the link protocol.

2.9.1 Starting Configuration

A protocol aware signal source and receiver such as a Protocol Test Card (PTC), Bit Error Rate Tester (BERT) or another specialized test equipment is connected to the device under test via a CLB. Since it is necessary to send commands to the DUT to adjust the transmitter equalization values and to get the DUT into loopback mode in order to perform this test, the protocol aware test equipment must be able to perform the sequence of steps outlined in the *PCI Express Base Specification*, and in this document's Appendix A: Getting into Loopback for 8GT/s & 16GT/s.

2.9.2 System Board Transmitter Link Equalization Response Test for 8.0 GT/s

The test is performed by following these steps:

1. Power down the system under test.
2. Insert the CLB revision 3.0 or 4.0 into the system under test.
3. Connect the transmitter output of the protocol aware test equipment to the Rx SMP connectors on the CLB lane under test via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
4. TX lanes other than the lane under test can be terminated with 50-ohm terminations or unterminated – as requested by the device under test provider.

5. Connect the Tx lane under test to signal splitters with one set of outputs going to the receiver inputs of the protocol aware test equipment and the other set of outputs going to a high-speed oscilloscope or equivalent data capture instrument (if the protocol aware test equipment is capable of acquiring the signal on its receiver and saving it to a file, the splitters and oscilloscope can be omitted). All connections to the CLB should be made via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables. All other connections should be made via phase matched, low loss SMA cables.
6. Connect SMP-SMA cables (or SMA-SMA cables with SMA-SMP adapters) from edge mounted Clock SMP's on CLB to the "Clock Input" pin on the data capture instrument. Clock multiplier setting on the data capture instrument may need to be adjusted to get the bit rate clock. If using revision 3.0 CLB, make sure that the Switches on the CLB are set correctly to route the clock from the card edge to the edge mounted SMP's. No switch setting is needed for revision 4.0 CLB.
7. Power on the system under test.
8. Have the test equipment train the DUT and negotiate to 8.0 GT/s.
9. Have the test equipment send a command to the DUT to set the transmitter to preset four (pre-shoot to 0.0dB and de-emphasis to 0.0dB).
10. Verify that the requested equalization change is complete within 1 microsecond from when the test equipment first sends the request. Note – the test equipment operator must be able to determine when the first request was sent relative to the observed TX EQ changed in the DUT.
11. Have the test equipment put the DUT into loopback and transmit the compliance pattern so that it gets returned to the test equipment and oscilloscope.
12. Capture 1.6 million unit-intervals of data ($1.6 \times 10^6 \times 125.0$ps = 200.0 µs). Save the captured waveform to a file with a unique name to identify that this waveform mimics preset four.
13. Repeat steps 6-11 with each additional preset from P0 to P9.
14. Use the SigTest Transmitter Preset Test option to read the saved waveform files and compute the preset values from these. All preset values computed must be within their specified limits.
15. The test is repeated with each request for the device under test TX equalization using the cursors reported by the system under test for that preset.

2.9.3 System Board Transmitter Link Equalization Response Test for 16.0 GT/s

> **Note:** The initial preset sent by the System is unknown. If the preset requested by the test equipment used for measuring the response time is the same as the initial preset or not different enough electrically as to allow a noticeable change to the voltage level on the scope, this preset does not require a response time measurement.

The test is performed using the following steps:

1. Power down the system under test.
2. Insert the CLB revision 4.0 into the system under test.
3. Connect the transmitter output of the protocol aware test equipment to the Rx SMP connectors *on the CLB lane under test via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.*
4. TX lanes other than the lane under test can be terminated with 50-ohm terminations or unterminated – as requested by the device under test provider.
5. Connect the Tx lane under test to signal splitters with one set of outputs going to the receiver inputs of the protocol aware test equipment and the other set of outputs going to a high-speed oscilloscope. All connections to the CLB should be made via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables. All other connections should be made via phase matched, low loss SMA cables.

   > **Note:** The variable ISI board is not used for this test.

6. Power on the system under test.
7. Have the test equipment train the DUT and negotiate to 16.0 GT/s.
8. Have the test equipment send a command to the DUT to set the transmitter to preset 0 (pre-shoot to 0.0dB and de-emphasis to -6.0dB).
9. Verify that the requested equalization change is complete within 1 microsecond from when the test equipment first sends the request. Note – the test equipment operator must be able to determine when the first request was sent relative to the observed TX EQ changed in the DUT.
10. Have the test equipment put the DUT into loopback and transmit the compliance pattern so that it gets returned to the test equipment and oscilloscope.
11. Capture 2.0 million unit-intervals of data (2.0 X 10^6 X 62.5ps = 125.0µs). Save the captured waveform to a file with a unique name to identify that this waveform mimics preset zero.
12. Repeat steps 6-11 with each additional preset from P1 to P9.

13. Use the SigTest Transmitter Preset Test option to read the saved waveform files and compute the preset values from these. All preset values computed must be within their specified limits.

14. The test is repeated with each request for the device under test TX equalization using the cursors reported by the system under test for that preset.

2.10 System Lane Margining at 16 GT/s

The System LMT tests whether the System under test implements the lane margining capability but the margin value reported is not checked against any traceable metric. This test is run on all card electromechanical form factor systems that operate at 16.0 GT/s. This test checks the on-die lane margining of a system using a Gold Add-in Card by adjusting the Transmitter signal quality (e.g. TX Preset, Vswing, channel loss, TX Jitter) and looking for a change in the timing margin and if applicable, voltage margin. If there is at least one Retimer present on the system under test, the lane margin test shall only be performed on the Retimer's receiver facing the CEM connector. This case will require knowledge of the Retimer's presence so the Lane Margin Tool can be configured to communicate to the indicated receiver using the appropriate protocol.

1. Insert the Gold Add-in Card into the system under test.
2. Power on the system under test.
3. Install Lane margining tool (LMT) on the system under test.
4. Train the system under test into L0 at 16 GT/s.
5. Use the Gold Add-in Card to change the TX signal sent to the system receiver under test. AIC TX parameters (e.g. TX Preset, Vswing, channel loss, TX Jitter) can be adjusted for this purpose.
6. Run the LMT on the system under test. Select system under test receiver or Retimer receiver, if applicable, for margin testing. Note down the reported Timing and, if applicable, Voltage margins.
7. Repeat steps 4 through 6 with by changing one of the AIC TX parameters listed in Step-5 and record timing and if applicable, Voltage margins.
8. If a noticeable change to the timing margin is observed between steps 6 and 7, the test is passed. If voltage margining is supported, a change should also be observed but is not required.
9. This test is run on Lane-0.

2.11 Add-in Card Receiver Link Equalization Test

This test is run on all card electromechanical form factor Add-in Cards that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the Add-in Card will correctly negotiate with its link partner to adjust the partner's transmitter equalization appropriately.

2.11.1 Starting Configuration, Overview of Calibration Steps at 8.0 GT/s

The calibration is performed by following these steps:

1. Connect the end of the cables that will connect to the RX SMPs on the test fixture as directly as possible (if any adaptors are used they must be minimal loss) to a real time oscilloscope and the other end to the test equipment generator and differential mode noise solution.
2. Have the test equipment transmit a pattern with 64 ones followed by 64 zeros followed by 128 bits of a 1010 clock pattern at 8 GT/s.
3. Measure the transmitted signal on the oscilloscope and adjust the post cursor de-emphasis and swing of the generator until the low frequency and high frequency portions of the signal have an equal differential amplitude of 800 mV peak-to-peak.
4. Adjust the Rj source of the test equipment to target approximately 1.5 ps RMS. The Rj is applied over the frequency range defined in the *PCI Express 3.0 Base Specification*.
5. Capture 1.6 million unit-intervals of data with a 1010 clock pattern ($1.6 \times 10^6 \times 125.0$ps = 200.0µs). Save the captured waveform to a file.
6. Analyze the waveform just captured using SigTest and the template PCIE_3_8GB_CEM_Rx_Sj_CAL.dat. Note the amount of spectrally flat Rj.
7. If the computed Rj is not within the calibration limits of 1.5 +.2/-0 ps RMS, readjust the Rj value on the generator accordingly and repeat steps 5 through 6. Note that Rj will be adjusted again in final adjustments to achieve the target eye height and width.
8. Note the Rj setting on the generator so that it can be recalled later.
9. Turn all jitter and noise sources off.
10. Have the test equipment transmit the Gen 3 compliance pattern with no noise or jitter sources turned on.
11. Capture 1.6 million unit-intervals of data ($1.6 \times 10^6 \times 125.0$ps = 200.0µs). Save the captured waveform to a file.
12. Analyze the waveform just captured using SigTest and the template PCIE_3_8GB_CEM_Rx_Sj_CAL.dat (does not apply the reference equalizer). Note the amount of Tj (total jitter) found by SigTest.

13. Adjust the 100 MHz Sj (sinusoidal jitter) component of the generator to approximately 0.1UI (12.5 ps).
14. Capture 1.6 million unit-intervals of data (1.6 X 10^6 X 125.0ps = 200.0µs). Save the captured waveform to a file.
15. Analyze the waveform just captured using SigTest and the template PCIE_3_8GB_CEM_Rx_Sj_CAL.dat. Note the amount of Tj. The amount of Sj is found by subtracting the Tj found in step 12 from the Tj just computed.
16. If the computed Sj is not within calibration limits of 12.5 +1/-0 ps, readjust the Sj value on the generator accordingly and repeat steps 14 through 15.
17. Note the Sj setting on the generator so that it can be recalled later.
18. Turn all jitter sources off.
19. Connect a revision 3.0 CLB to a revision 3.0 CBB without power
20. Connect the generator output to the Rx lane 0 SMP connectors on the CBB using the same cables used in calibration (if any adaptors are also used they must be minimal loss).
21. Connect the lane 0 Tx SMP connectors on the CLB to a high-speed oscilloscope via SMP to SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP to SMA cables.
22. Set the generator output to an all zero pattern and turn the generator output on. Adjust the 2.1 GHz differential noise component of the test equipment output to approximately 20 mV. Measure the DM average peak to peak amplitude over 1.6 X 10^6 unit intervals (at 8 GT/s) and adjust it to the range of 14-16 mv. Note that DM will be adjusted again in the final adjustments to achieve the target eye height and width.

> Note: A high quality power supply should be used to power the CBB as lower quality supplies have been known to artificially inflate the DMI calibration measurements leading to a pessimistic test or other unexpected behaviors.
>
> Note the differential noise setting on the test equipment so that it can be recalled later.

23. Connect the end of the phase matched, low loss SMA cables (connected to the test equipment source and differential mode noise solution) directly to a real time oscilloscope.
24. Adjust the TX equalization of the test equipment so the measured TX equalization on the oscilloscope is P7. Measured pre-shoot must be 3.5 +/- .2 dB and measured de-emphasis must be 6.0 +/- .2 dB.

25. **For Add-in Cards:** Connect the test equipment transmitter output to the Rx Lane 0 SMP connectors on the CBB 3.0 via SMP-to-SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP-to-SMA cables.
    For systems: Connect the test equipment transmitter output to the Rx Lane 0 SMP connectors on the CLB 3.0 via SMP-to-SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP-to-SMA cables.
26. **For Add-in Cards**: Connect the Lane 0 Tx SMP connectors on the CLB 3.0 to a high-speed oscilloscope or equivalent data capture instrument via SMP-to-SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP-to-SMA cables.
    For systems: Connect the Lane 0 Tx SMP connectors on the CBB 3.0 to a high-speed oscilloscope or equivalent data capture instrument via SMP-to-SMA adaptors and phase matched, low loss SMA cables or phase matched, low loss SMP-to-SMA cables.
27. Set all jitter and noise sources to the calibration values found above and have the test equipment transmit TX compliance pattern.
28. Capture 1.6 million unit-intervals (1.6 X 10^6 X 125.0ps = 200.0 µs) of data with the real time oscilloscope. Save the captured waveform to a file.
29. Analyze the waveform just captured using SigTest template "PCIE_3_8GB_CEM_Rx_SYS_CAL" for system testing and template "PCIE_3_8GB_CEM_Rx_CARD_CAL" for AIC testing, including embedding the remaining portion of the appropriate channel.
30. Note the eye height and eye width.
31. Adjust the test equipment source Rj and/or DMI until the measured eye height over an average of three measurements is:
    - For Add-in Cards: 46 mV +0/-5 mV
    - For systems: 50 mV +0/-5 mV

    The measured eye width over an average of three measurements is:
    - For Add-in Cards: 41.25 +0/-2 ps
    - For systems: 45ps +0/-2 ps.

> **Note:** It is preferable to get as close to the nominal values of 46 mV and 41.25 ps for Add-in Cards or 50 mV and 45 ps for systems as possible.

2.11.2 Overview of Calibration Steps at 16.0 GT/s

For this calibration a real time oscilloscope with the bandwidth limited to 25 GHz (maximum bandwidth must be greater than or equal to 25 GHz) and a minimum sample rate of 64 GS/s.

The calibration is performed by following these steps:

1. Connect the end of the cables that will connect to the RX SMPs on the test fixture as directly as possible (if any adaptors are used they must be minimal loss) to a real time oscilloscope and the other end to the test equipment generator and differential mode noise solution. The differential mode noise solution may be internal to the test equipment generator.
2. Have the test equipment transmit a pattern with 64 ones followed by 64 zeros followed by 128 bits of a 1010 clock pattern at 16 GT/s.
3. Measure the transmitted signal on the oscilloscope and adjust the post cursor de-emphasis and swing of the generator until the low frequency and high frequency portions of the signal have an equal differential amplitude of 800 mV peak to peak.
4. Repeat step 3 for 720 mV peak to peak and record the value.
5. Change the de-emphasis and swing of the generator back to the calibrated values for 800 mV peak to peak.
6. Adjust the Rj source of the test equipment to target approximately 1.0 ps RMS. The Rj is applied over the frequency range defined in the PCI Express 4.0 Base Specification. Enable 100 MHz Sj and 2.1 GHz DMI but set the magnitude to 0.0ps and 0.0mV respectively.
7. Capture 2.0 million unit-intervals of data with a 1010 clock pattern (2.0 X 10^6 X 62.5ps = 125.0µs). Save the captured waveform to a file.
8. Analyze the waveform just captured using SigTest and the template for Gen 4 Rj calibration (PCIE_4_0_RX_CAL \ PCIE_4_16GB_CEM_Rj_Sj_CAL.dat). Note the amount of spectrally flat Rj.
9. If the computed Rj is not within the calibration limits of 1.0 +.1/-0 ps RMS, readjust the Rj value on the generator accordingly and repeat steps 6 through 8.
10. Note the Rj setting on the generator so that it can be recalled later.
11. Turn all jitter and noise sources off.
12. Optimally enable 100 MHz Sj, Rj, & 2.1 GHz DMI but set the magnitude to 0.0ps, 0.0ps, and 0.0mV respectively. If any of these sources have a non-zero minimum setting, disable the jitter or noise source(s).
13. Capture 2.0 million unit-intervals of data (2.0 X 10^6 X 62.5ps = 125.0µs). Save the captured waveform to a file.
14. Analyze the waveform just captured using SigTest and the template for Sj calibration (PCIE_4_0_RX_CAL \ PCIE_4_16GB_CEM_Rj_Sj_CAL.dat - does not apply the reference equalizer). Note the amount of Max Peak to Peak Jitter (ps) found by SigTest.

15. Adjust the 100 MHz Sj (sinusoidal jitter) component of the generator to approximately 0.1UI (6.25ps).
16. Capture 2.0 million unit-intervals of data (2.0 X 10^6 X 62.5ps = 125.0µs). Save the captured waveform to a file.
17. Analyze the waveform just captured using SigTest and the template for Gen 4 Sj calibration. Note the amount of Max Peak to Peak Jitter (ps). The amount of Sj is found by subtracting the Max Peak to Peak Jitter (ps) found in step 14 from the Max Peak to Peak Jitter just computed.
18. If the computed Sj is not within calibration limits of 6.25 +0.5/-0 ps, readjust the Sj value on the generator accordingly and repeat steps 16 through 17. Note that Sj will be adjusted again in the final adjustments to achieve the target eye height and width.
19. Note the Sj setting on the generator so that it can be recalled later.
20. Repeat steps 15 through 19 to calibrate Sj to 5 +0.5/-0 ps & 10 +0/-0.5ps.
21. Turn all jitter and noise sources off.
22. Adjust the TX equalization of the test equipment so the measured TX equalization on the oscilloscope is P5. Measured pre-shoot must be 1.9 +/- .1 dB and measured de-emphasis must be 0.0 +/- .1 dB.
23. Adjust the TX equalization of the test equipment so the measured TX equalization on the oscilloscope is P6. Measured pre-shoot must be 2.5 +/- .1 dB and measured de-emphasis must be 0.0 +/- .1 dB.

> **Note:** For calibration of the stressed eye at 16 GT/s only P5 & P6 are required. For the Add-in Card Receiver Link Equalization Test for 16 GT/s and the System Board Receiver Link Equalization Test for 16 GT/s P0 through P9 must all be calibrated. This would be a convenient time to perform the calibrations of P0, P1, P2, P3, P4, P7, P8, and P9.

24. Note the TX equalization settings on the generator so that it can be recalled later.
25. Connect a revision 4.0 CLB to a revision 4.0 CBB without power
26. Using a VNA or equivalent method to measure Insertion Loss, determine which lanes on the Variable ISI board can be used to achieve a 27 dB, 28 dB and 30 dB channel – See Appendix C.
27. Connect the generator and scope to the 28dB channel (use the same SMA cables from the earlier calibration steps)
    a) Add-in Card Rx Calibration Channel: Generator→SMA Cable→SMA to SMP Adaptor→ Variable ISI Board (Pair established in Appendix C) →CBB→CLB→Variable ISI Board (Pair established in Appendix C) → SMP to SMA Adaptor→SMA Cable→Scope (3dB package embedding).
       The 3dB package model (refpkg_endpoint_3db_thru.s4p) can be found in the Sigtest Package (Ver 4.0.45) located here.
    b) System Rx Calibration Channel: Generator→SMA Cable→SMA to SMP Adaptor→ Variable ISI Board (Pair established in Appendix C) →SMP Cable→CLB→CBB→SMP Cable→ Variable ISI Board (Pair established in Appendix C) → SMP to SMA Adaptor→SMA Cable→Scope (5dB package embedding). The 5dB package model (refpkg_rootcomplex_5db_thru4p.s4p) can be found in the Sigtest Package (Ver 4.0.45) located here.

28. Set the generator output to an all zero pattern and turn the generator output on.
29. Adjust the 2.1 GHz differential noise component of the test equipment output to approximately 14 mV.
30. Measure the DMI RMS amplitude over 40 ns with a maximum sample interval of 15.625 ps (64 GS/s) and adjust it to the range of 14 +0/-2 mV after converting from RMS to Differential Amplitude. Note that DMI will be adjusted again in the final adjustments to achieve the target eye height and width.
31. Note the DMI setting on the test equipment so that it can be recalled later.
32. Repeat steps 29 through 30 to calibrate DMI to 10 mV and 25 mV.
33. Set the generator output to an all zero pattern and turn the generator output on.
34. Adjust the 120 MHz common mode noise (CMI) component of the test equipment output to approximately 150 mV.
35. Measure the CMI RMS amplitude over 2.0 million unit-intervals of data (2.0 X 10^6 X 62.5ps = 125.0µs) and adjust it to the range of 150 +0/-2 mV after converting from RMS to Differential Amplitude. Note that CMI will be disabled during the stressed eye calibration but enabled for the receiver link equalization test.

> **Note:** A high quality power supply should be used to power the CBB as lower quality supplies have been known to artificially inflate the DMI calibration measurements leading to a pessimistic test or other unexpected behaviors.

36. Note the CMI setting on the test equipment so that it can be recalled later.
37. Connect the generator and the scope to the 27dB channel (use same SMA cables from earlier calibration steps). This is achieved by changing the Variable ISI pairs (See Appendix C).
38. Set jitter and noise sources as follows: Rj is set to 1ps RMS, Sj is set to 0.1UI, DMI is set to 14mV, and CMI will be enabled but set to 0.0 mV if the signal generator is capable of this setting, otherwise have CMI disabled. Set the TX Equalization to Preset 5 and have the test equipment transmit TX compliance pattern.
39. Capture seven 2.0 million unit-interval waveforms (2.0 X 10^6 X 62.5 ps = 125.0 µs) with a real time oscilloscope and save to separate files.
40. Change the TX Equalization setting to Preset 6.
41. Capture seven 2.0 million unit-interval waveforms (2.0 X 10^6 X 62.5 ps = 125.0 µs) with a real time oscilloscope and save to separate files.
42. Analyze the waveforms just captured using SigTest with the Rx Calibration template files (PCIe_4_16G_Rx_CAL_CTLE_8dB.dat up to and including PCIe_4_16G_Rx_CAL_CTLE_11dB.dat) . The CTLE range from 8.5 dB to 10.5 dB in ¼ dB step sizes is run for every P5 and P6 waveform.

43. Report the average Minimum Eye Width & Extrapolated Eye Height (both at E-12) for P5 & P6 with the optimal CTLE.
    a) All waveform outliers are removed from the average
        - If the Eye Width is less than 1.0 ps or deviates from the median by 5.0 ps the waveform is considered an outlier.
        - If the Eye Height is less than 1.0 mV or deviates from the median by 8.0 mV the waveform is considered an outlier.
    b) If most of the waveforms captured meet the outlier criteria with the 27dB channel, there is likely an issue with the generator or channel.
44. Find which Preset & CTLE combination gives the largest Eye Area (Eye Width * Eye Height) and record these values.
45. If the Extrapolated Eye Height is above 15 mV and the Minimum Eye Width is above 18.75 ps increase the loss of the variable ISI board by 0.5dB (not exceeding the 30 dB channel from step 26).
46. Repeat steps 27 through 42 if the eye width and height are still above the targets. Once either the eye width or the eye height drops below the target, step back to the previous channel. This becomes the final calibration channel
47. Adjust the test equipment source Sj, DMI, & Swing within the limits defined until the measured Extrapolated Eye Height is 15 +1.5/-1.5 mV and the measured Minimum Eye Width is 18.75 +0.5/-0.5 ps.

> **Note**: It is preferable to get as close to the nominal values of 15 mV and 18.75 ps as possible.
>
> Adjustment of Differential Voltage Swing is optional and not required if the target eye width and eye height can be achieved by adjusting Sj and DMI only:
> - Sj – 5 to 10 ps PP @ TP1
> - DMI – 10 to 25 mV PP @ TP2
> - Differential Voltage Swing – 720 to 800 mV PP @ TP1
>
> Refer to the *PCI Express Base Specification* for definitions of TP1 and TP2.

48. For each Sj, DMI, and Swing explored, twenty 2.0 million unit-interval waveforms ($2.0 \times 10^6 \times 62.5$ ps = 125.0 µs)are captured and processed with SigTest using the optimal CTLE established in step 39. The outlier removal defined in step 43a is required for this final tuning.

2.11.3 Add-in Card Receiver Link Equalization Test for 8.0 GT/s

The test is performed by following these steps:

1. Insert the Add-in Card under test into the calibration revision 3.0 CBB without power. The signal source should be connected to the Rx lane under test on the CBB riser card, the receiver of the protocol aware test equipment should be connected to the Tx lane under test on the CBB main board. Other TX lanes can be terminated with 50-ohm terminations or unterminated – as requested by the device under test operator.
2. Configure the protocol aware test equipment transmitter to initially transmit with preset P7 at 8.0 GT/s.
3. Power on the CBB.
4. Have the protocol aware test equipment train the DUT and negotiate to 8.0 GT/s.
5. Have the protocol aware test equipment run the link equalization protocol.
6. Have the protocol aware test equipment put the DUT into loopback.
7. Send the modified compliance pattern to the device under test
8. Verify that the error detector found no more than one errors in 10^{12}bits transmitted.
9. Repeat the test with the protocol aware test equipment configured to initially transmit with preset P8 at 8 GT/s.

2.11.4 Add-in Card Receiver Link Equalization Test for 16.0 GT/s

The test is performed by following these steps:

1. Insert the Add-in Card under test into the calibration revision 4.0 CBB without power. The signal source should be connected to the Rx lane under test on the CBB riser card, the receiver of the protocol aware test equipment should be connected to the Tx lane under test on the CBB main board. Other TX lanes can be terminated with 50-ohm terminations or unterminated – as requested by the device under test operator.
2. The protocol aware test equipment will initially transmit the preset requested by the Add-in Card at 16.0 GT/s. If there is no request from the add-in card, configure to initially transmit with preset P7 at 16.0 GT/s.
3. Power on the CBB.
4. Have the protocol aware test equipment train the DUT and negotiate to 16.0 GT/s.
5. Have the protocol aware test equipment run the link equalization protocol.
6. Have the protocol aware test equipment put the DUT into loopback.
7. Send the modified compliance pattern to the device under test
8. Verify that the error detector found no more than one errors in 1012bits transmitted.

2.12 System Receiver Link Equalization Test

This test is run on all card electromechanical form factor systems that operate at 8.0 GT/s and 16.0 GT/s. The test verifies that the system will correctly negotiate with its link partner to adjust the partner's transmitter equalization appropriately.

2.12.1 Starting Configuration, Overview of Calibration Steps at 8.0 GT/s

Perform steps 1-32 from Section 2.11.1.

2.12.2 Overview of Calibration Steps at 16.0 GT/s

Perform steps 1-48 Section 2.11.2.

2.12.3 System Board Receiver Link Equalization Test for 8.0 GT/s

1. Insert the calibration revision 3.0 CLB into the system under test without power. The signal source should be connected to the Rx lane under test on the CLB, the receiver of the protocol aware test equipment should be connected to the Tx lane under test on the CLB. The CLB 100 MHz clock output from the system under test shall be connected to the test equipment and drive the test equipment transmissions after being filtered by a *PCI Express Base Specification* compliant PLL or equivalent. Other TX lanes can be terminated with 50-ohm terminations or unterminated – as requested by the device under test operator.
2. Configure the protocol aware test equipment transmitter equalization to match the initial TX EQ preset at 8 GT/s requested by the system board under test. This can be observed using separate protocol analysis equipment if necessary.
3. Power on the system under test.
4. Have the protocol aware test equipment train the DUT and negotiate to 8.0 GT/s.
5. Have the protocol aware test equipment run the link equalization protocol.
6. Have the protocol aware test equipment put the DUT into loopback.
7. Send the modified compliance pattern to the device under test.
8. Verify that the error detector found no more than one error in 10^{12} bits transmitted.

2.12.4 System Board Receiver Link Equalization Test for 16.0 GT/s

1. Insert the calibration revision 4.0 CLB into the system under test without power. The signal source should be connected to the Rx lane under test on the CLB, the receiver of the protocol aware test equipment should be connected to the Tx lane under test on the CLB. The CLB 100 MHz clock output from the system under test shall be connected to the test equipment and drive the test equipment transmissions after being filtered by a *PCI Express Base Specification* compliant PLL or equivalent. Other TX lanes can be terminated with 50-ohm terminations or unterminated – as requested by the device under test operator.
2. Configure the protocol aware test equipment transmitter equalization to match the initial TX EQ preset at 16.0 GT/s requested by the system board under test. This can be observed using separate protocol analysis equipment if necessary.
3. Power on the system under test.
4. Have the protocol aware test equipment train the DUT and negotiate to 16.0 GT/s.
5. Have the protocol aware test equipment run the link equalization protocol.
6. Have the protocol aware test equipment put the DUT into loopback.
7. Send the modified compliance pattern to the device under test.
8. Verify that the error detector found no more than one error in 10^{12} bits transmitted.

2.13 Add-in Card PLL Bandwidth

This test is run on all card electromechanical form factor Add-in Cards. The test verifies that the Add-in Card PLL bandwidth and peaking are within the limits allowed by the PCI Express specifications.

2.13.1 Starting Configuration

1. Connect one of the following two options to provide a reference clock with modulation for the PLL bandwidth test:
   a) Connect a signal generator to the noise injection port on the CBB. Note that the CBB may need to be modified to enable the port.
   The signal generator must be able to provide a signal that induces phase jitter on the reference clock from 0 to 25 MHz.

   > **Note:** This approach will work with PLL designs that use only the rising edge of the reference clock.

   b) Connect an external source to the CBB reference clock input.
   The external source must be able to provide a 100 MHz reference clock signal with phase jitter from 0 to 25 MHz.

   > **Note:** This approach works with PLL designs that use both edges of the reference clock or only the rising edge of the reference clock.

2. Connect the output of transmit lane zero on the CBB main board to an instrument capable of measuring the transmitter frequency response as a function of the frequency of phase jitter on the reference clock.

2.13.2 Overview of Test Steps

The test is performed by following these steps:

1. Insert the Add-in Card under test into the CBB with the power off.

> **Note:** If this test is performed at 8 GT/s the 3.0 CBB or 4.0 CBB must be used. If this test is performed at 16 GT/s the 4.0 CBB must be used.

2. Make sure that the compliance toggle outputs (SMP connectors J5 and J85) on the CBB main board are connected to receive lane zero (SMP connectors J18 and J2) on the CBB riser card via appropriate SMP to SMP cables.
3. Power on the CBB.
4. Push the compliance toggle button on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the Add-in Card under test) until the compliance pattern at the desired data rate and with the desired Tx EQ preset is selected.
5. Measure the transmitter output and confirm the transmitter output is the compliance pattern at the desired data rate.
6. Apply modulation on the reference clock producing phase jitter from 0 to 25 MHz. The modulation reference clock is calibrated such that the measured reference clock phase jitter is within the following ranges:
   a) Reference clock phase jitter at 2.5 GT/s: 40.0 +0/-20% ps peak-to-peak
   b) Reference clock phase jitter at 5.0 GT/s: 20.0 +0/-20% ps peak-to-peak
   c) Reference clock phase jitter at 8.0 GT/s: 13.0 +0/-20% ps peak-to-peak
   d) Reference clock phase jitter at 16.0 GT/s: 7.0 +0/-20% ps peak-to-peak
7. Analyze the transmitter output and estimate the reference clock phase jitter frequency where the transmitter response is -3 dB. Also note the maximum phase jitter amplitude of the transmitter output for determining the peaking value.
8. The -3 dB point must fall between the frequencies specified for the current data rate and the maximum peaking must be less than maximum allowed peaking for the current data rate. When testing is done at PCI-SIG compliance workshops a relaxation of ±0.5 MHz on bandwidth limits and + 0.25 dB on the peaking are allowed against the specified pass/fail value to allow for test equipment variation.
9. Repeat steps 4-7 with the amplitude set to ½ of the initial calibrated noise amplitude value.

10. Push the compliance toggle button on the CBB (inject a 1 ms pulse of a 100 MHz clock signal into receive lane zero of the Add-in Card under test) to move to the desired data rate and the desired TX EQ Preset. on next data rate supported by the add-in card.
11. Repeat steps 4-9 until all data rates supported by the Add-in Card have been tested. For testing at 8 GT/s and 16 GT/s start with Preset 7 but testing with other presets are allowed. A passing result with any preset is sufficient to pass this test.

2.14 Add-in Card PCB Impedance (informative)

This test is run on all card electromechanical form factor add-in cards. The test verifies that the Add-in Card TX and RX path PCB differential trace impedance is in the range required by the PCI Express 3.0 Card Electromechanical Specification.

The differential impedance of the Tx and Rx lanes is checked with a TDR or equivalent to verify that the measured impedance of the PCB trace only (package is excluded) is within the CEM specification.

2.15 System Board PCB Impedance (Informative)

This test is run on all card electromechanical form factor system boards. The test verifies that the system board TX and RX path PCB differential trace impedance is in the range required by the PCI Express 3.0 Card Electromechanical Specification.

The differential impedance of some or all the Tx and Rx lanes is checked with a TDR or equivalent to verify that the measured impedance of the PCB trace only is within specification.

A

Appendix A. Getting into Loopback

To perform receiver tolerance tests the product under test must first be trained and directed to enter the Loopback state. This is done by taking the product through the state machine from Detect via Polling and Configuration to the Loopback state using the protocol as specified in PCI Express Base Specification, Rev 2.0.

A.1 Loopback Training

The state transitions needed to get the device under test into loopback mode shown in Figure 1.

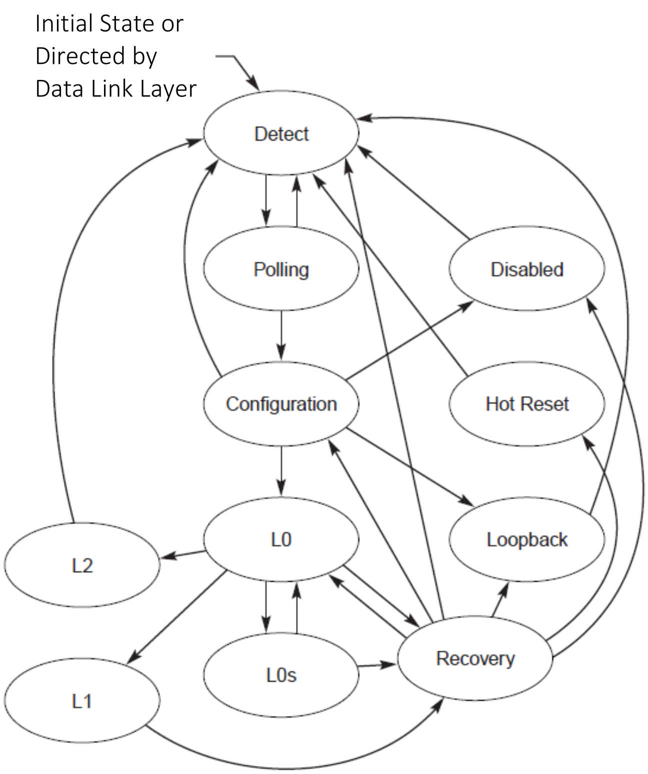

Figure 1. Main State Diagram for Link Training and Status State Machine

A.2 Step by Step Sequence

The following sequence of steps will cause the device under test to enter loopback state:

1. Start sending TS1 with PAD (K23.7) which takes the product into the Polling.Active state (Figure 2).

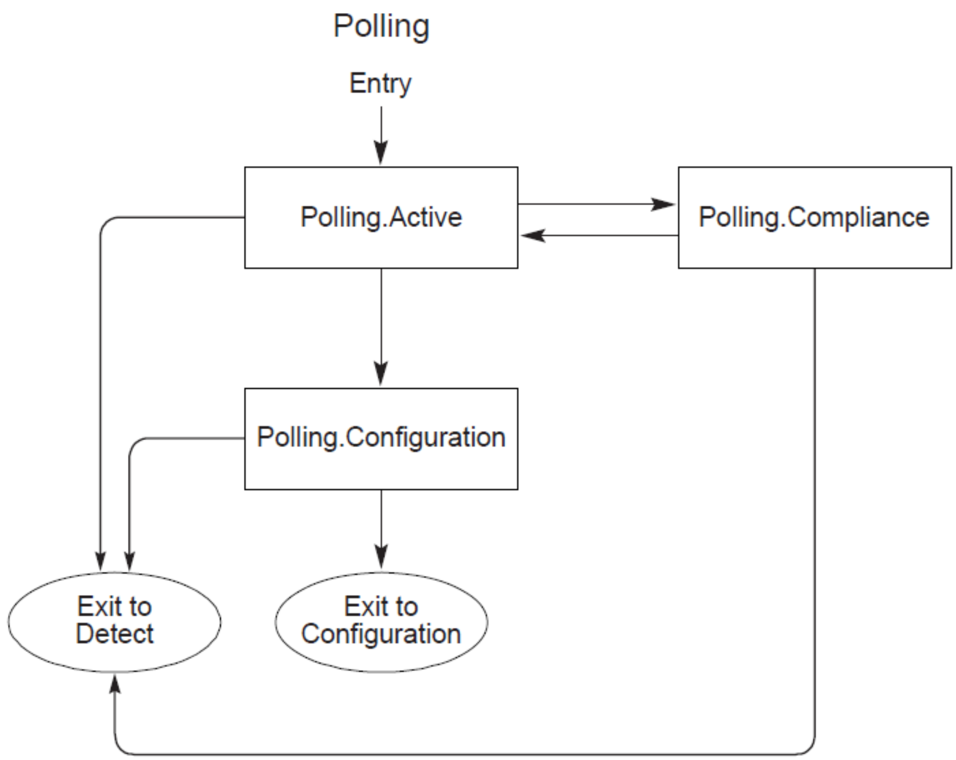

Figure 2. Polling Sub-State Machine

2. Polling.Configuration is reached after >1024 TS1 have been transmitted and 8 consecutive TS1 or TS2 with Pad or Loopback bit asserted have been received.
3. The Configuration state is entered after 8 consecutive TS2 with Pad have been received and 16 TS2 have been transmitted after 1 TS2 has been received.
4. Speed negotiation is initiated by sending TS1 at 2.5 GT/s advertising the supported speeds.
5. Electrical idle for more than 1 ms allows the product to adjust to the requested speed unless the requested speed is 2.5 GT/s.
6. Two consecutive TS1 at the requested speed with Loopback bit asserted takes the product to the Loopback state.

A.2.1 Loopback Training at 2.5 GT/s

The sequence necessary to cause a device under test to enter loopback at a data rate of 2.5 GT/s is shown in Figure 3.

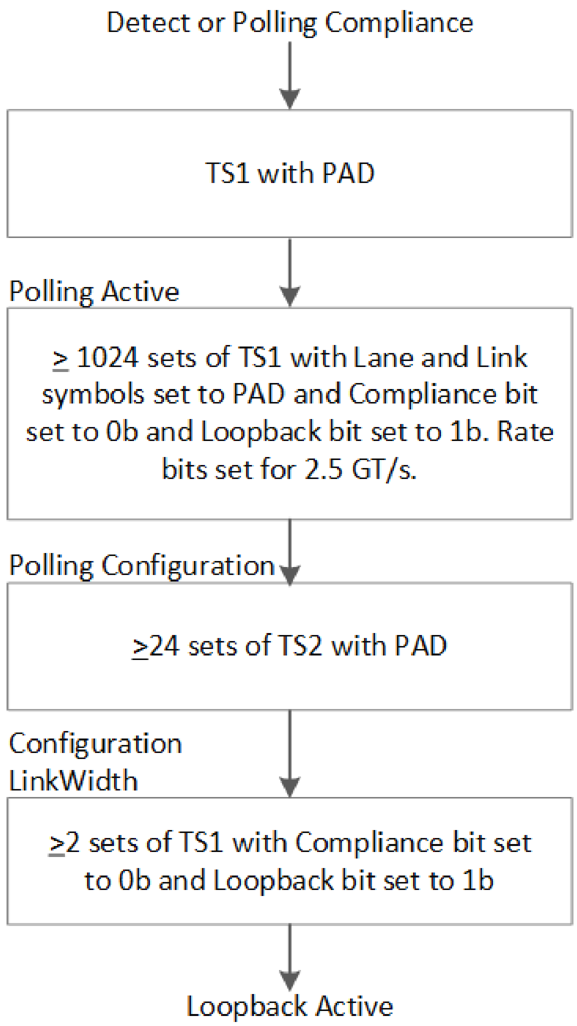

Figure 3. 2.5 BT/s Loopback Training Sequence

A.2.2 Loopback Training at 5.0 GT/s

The sequence necessary to cause a device under test to enter loopback at a data rate of 5.0 GT/s is shown Figure 4.

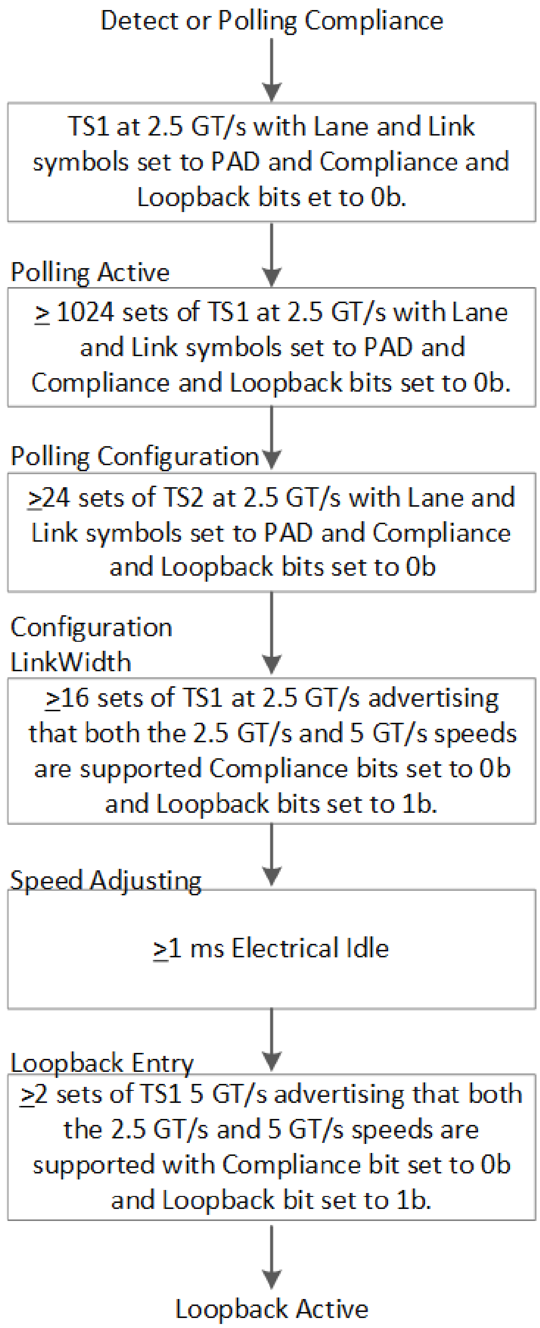

Figure 4. 5.0 GT/ s Loopback Training Sequence

A.2.3 Loopback Training at 8.0 GT/s

The sequences that will be used to cause a device under test to enter loopback through the configuration link state and through the recovery link state at a data rate of 8.0 GT/s are specified in the *PCI Express 3.0 Link Test Specification*.

B

Appendix B. Transmitter Signaling Analysis

The process of analyzing transmitter output to determine the signal quality and, ultimately, the ability of a transmitter to operate with any receiver that complies with the receiver specification is an intricate process. While the Dual Dirac method used in this analysis is well documented elsewhere, it is useful to describe this analysis technique as used for transmitter testing here.

B.1 Outline of Tx Signal Analysis

Within the context of PCI Express, transmitter electrical compliance is computed by analyzing a waveform captured using a high-speed, real time oscilloscope. Because of the high frequency nature of the signal being analyzed, the oscilloscope must have a bandwidth of at least 6 Ghz and a sample rate of at least 20 GS/s (50 ps sample interval) for 2.5 GT/s signaling and a bandwidth of at least 12 Ghz and a sample rate of at least 40 GS/s (25 ps sample interval) for 5.0 GT/s and 8.0 GT/s signaling and a bandwidth of at least 25 Ghz and a sample rate of at least 80 GS/s (12.5 ps sample interval) for 16.0GT/s.

The captured waveform is optionally conditioned by a specified test channel and specified receiver equalization (CTLE and DFE). The resulting waveform is then analyzed for timing jitter and minimum and maximum signal amplitude.

Timing analysis is based on a specified target Unit Interval (UI) and, when doing random jitter (Rj) and deterministic jitter (Dj) separation, timing uncertainty extrapolated to a Bit Error Rate (BER) than can be significantly greater than the BER computed directly from the measured data.

Signal amplitude analysis is based on the measured waveform amplitude as modified by any specified waveform conditioning (test channel embedding and Rx equalization) and related to timing defined by the specified target UI.

B.2 Input Waveform Conditioning

Three different forms of waveform conditioning can be applied to the input waveform.

B.2.1 Channel Embedding

The channel is defined by S-Parameters. The channel description is read in and stored internally. When a waveform is presented for processing, the waveform is converted to the frequency domain then multiplied with the channel description. The result of the multiplication is converted back to the time domain.

The waveform is input as two single-ended acquisitions or a single differential acquisition and output as a single, differential waveform.

B.2.2 CTLE Equalization

Continuous Time Linear Equalization (CTLE) is performed in a similar manner to Channel Embedding. The input waveform is transformed into the frequency domain. The CTLE parameters (AC/DC gain, one zero frequency and two pole frequencies) are used to define an equivalent frequency domain response and the input waveform is convolved with the CTLE response. The result of the convolution is converted back to the time domain.

Multiple CTLE parameter sets can be specified. The waveform resulting from each CTLE filter then has DFE applied. The optimal CTLE (and, if specified, DFE) parameter set is determined by examining the resulting transition and non-transition eye heights and widths for each set of CTLE parameters. Once the optimal CTLE (and DFE, if specified) parameter set has been determined, it is applied to the entire waveform.

B.2.3 DFE Equalization

Decision Feedback Equalization (DFE) is performed strictly in the time domain. The eye area is used to find the optimal DFE tap value between – 30 and + 30 mV (inclusive). Once the taps are known, each sample point of the input waveform is modified according to the tap values and the state (logic 0 or logic 1) of the waveform at each tap location.

B.2.4 Crossover and Interval Determination

Once the input waveform conditioning has been performed, the input waveform is analyzed to determine the time at which the signal crosses the zero Volts threshold. The crossover time is determined using linear interpolation between the two sample points closest to the zero crossing.

The interval between successive crossovers is computed by subtracting the crossover time at the beginning of the interval from the crossover time at the end of the interval: Interval = Crossover*n*+1 – Crossover*n*. Information allowing a given interval to be traced back to its location within the input waveform is retained.

In most cases, (all cases except when the input waveform is a toggle pattern) the input waveform will contain multi-bit intervals. To meet the analysis requirements, the multi-bit intervals need to be replaced with multiple single bit intervals. The period of each added interval is merely the period of the original, multi-bit interval divided by the number of unit intervals represented.

Since this step is where the bit length of each interval is determined, any pattern checks that have been specified are performed at this time.

B.2.5 Time Interval Error (or Phase Jitter) Determination

The jitter per edge and the subsequent Time Interval Error (TIE) are computed based on the clock period for each unit interval in the input data. For single port measurements (as used in Add-in Card analysis) a single clock value is computed for the entire data record. For dual port analysis (as used in System Board analysis) the clock for each unit interval in the data record is computed from the supplied clock waveform. These methods are described below.

B.2.6 Single Port (Add-In Card) Jitter Determination

No explicit clock information is provided for single port analysis, so the clock must be determined from the data waveform. Two methods are available for doing this, least squares fit and mean interval.

B.2.6.1 Least Squares Fit Clock Interval Method

The least squares fit method plots the interval duration on the Y axis against the interval on the X axis. The least squares fit line is computed and the slope of this line is used as the unit interval period for jitter determination.

B.2.6.2 Mean Clock Interval Method

The mean interval method merely finds the mean of all the intervals and uses this value as the unit interval period for jitter determination.

B.2.6.3 Single Port Data Waveform Phase Jitter Computation

The jitter at each interval is found by subtracting the unit interval period (as computed above) from each interval. It is important to note that the resulting jitter value can be either positive (interval is greater than unit interval) or negative (interval is less than unit interval).

Finally, this jitter data is converted into phase jitter or the Time Interval Error (TIE) by accumulation; that is, the jitter at each unit interval is summed to give the TIE at that UI:

TIE0 = J0, TIEn = TIEn-1 + Jn.

B.2.6.4 Dual Port (System Board) Jitter Determination

For dual port analysis, the system clock is captured simultaneously with the data. Both the clock waveform and the data waveform are input to the analysis software and the data waveform is processed as described above in sections 4.1.1 through 4.1.2.

The clock waveform is processed in a similar manner, but without any waveform conditioning. Further, in general, the crossover times of only the rising edge of the clock waveform are interpolated. The resulting crossover periods (from rising edge to rising edge of the clock signal) are then interpolated to the correct number of unit intervals.

At this point, there is an array of unit interval values for the data and an array of unit interval value for the clock.

B.2.6.5 Phase-Locked Loop (PLL) Filter of Clock Jitter

Several different PLL filter values are specified to constrain the effect of the transmit and receive PLLs on the clock. For each specified filter value, the clock values are filtered according to each set of PLL filter parameters. The jitter values are computed for each filter specified and the total jitter (Tj) is used to determine which results to retain. The largest Tj found is retained as the result for all clock filter values.

B.2.6.6 Clock to Data Skew

Even though the clock waveform is captured simultaneously with the data waveform, there may be delay between the clock and data waveforms due to different routing on the system board. The CEM spec defines a maximum for this skew. To compensate for this possible skew, the analysis is done at three different values of clock to data skew:

- Clock delayed by maximum allowed amount with respect to the data.
- No delay introduced between clock and data.
- Data delayed by maximum allowed amount with respect to the clock.

Obviously, any delay must be an integer number of unit intervals so the number of unit intervals closest the specified maximum skew is used to offset the clock and data values.

As with the PLL filter values, the total jitter is computed for all three delay combinations and the worst case Tj is retained as the result. If there are three filters specified there will be three skew cases for each filter thus the algorithm to find the total jitter will be executed nine times in all.

B.2.6.7 Dual Port Data Waveform Phase Jitter Computation

The jitter at each interval is found by subtracting the clock interval from the data interval. The clock interval has been filtered (as noted in section 4.1.3.6 above) and clock to data skew has been applied (as noted in section 4.1.3.7 above). The phase jitter or Time Interval Error (TIE) is computed as described for the single port data waveform jitter in section 4.1.3.4 above.

B.2.6.8 Jitter Determination

The phase jitter, whether computed using the single port or dual port method, is used to compute the total jitter and, by application of the Dual Dirac method, the deterministic jitter.

B.2.6.9 Phase Jitter High Pass Filter

A high pass filter is applied to the phase jitter based on parameters specified. The filter can be a brick wall filter or a simple first or second order filter. The cut-off frequency, damping factor (for second order filters) and brick wall floor value (for brick wall filters) are specified for this filter.

B.2.6.10 Jitter Metrics

At this point, the total jitter for each unit interval represented in the input waveform is known. Jitter metrics such as maximum peak-to-peak jitter are computed and saved for display later.

B.2.6.11 Dual Dirac Fitting

With the suitably filtered jitter values available, first the Probability Distribution Function (PDF) then the left and right Cumulative Distribution Functions are computed. The PDF is found by forming a histogram of the jitter values around zero; the number of bins to be used in the histogram is supplied as a parameter to this function. The range of jitter values determines the size of each bin in picoseconds.

The cumulative distribution functions are found by accumulating the PDF from one end to the other. The left side CDF is generated by accumulating the PDF from left to right (index 0 through index n), the right-side CDF is generated by accumulating the PDF from the right to the left (index n through 0).

The left and right CDF values are converted to Q space using the complementary inverse error function. Specifically, the CDF is multiplied by two, converted by the complementary inverse error function then multiplied by the square root of two. The complementary inverse error function has the interesting property of mapping a Gaussian distribution into a straight line. Therefore, a Gaussian can be extrapolated in Q space merely by extending a straight line. This is done for both left and right cumulative distribution functions using a slope (Rj) computed from the frequency domain phase jitter.

C

Appendix C. PCIe 4.0 Electrical Test Fixture Characterization

C.1 Vector Network Analyzer (VNA Based Test Fixture Characterization

- PCIe TX signal quality test at 16 GT/s
- PCIe RX calibration at 16 GT/s
- PCIe Link Equalization RX test at 16 GT/s

See Figure 5.

C.2 Selection of Variable ISI Parts

- VNA measurements are used to select a variable ISI pair(s) that provide the correct amount of differential insertion loss (IL) at 8 GHz for each test
- All measurements referencing IL are assumed differential insertion loss (SSD3) at 8 GHz
- The VNA must have a minimum bandwidth of 8 GHz for this characterization

See Figure 6.

C.3 Inclusion of Coaxial Cables and Adapters

- Characterization is performed with coaxial cables and adapters
- The variable ISI pair selection comprehends the loss of coaxial cables and adapters used in the electrical tests

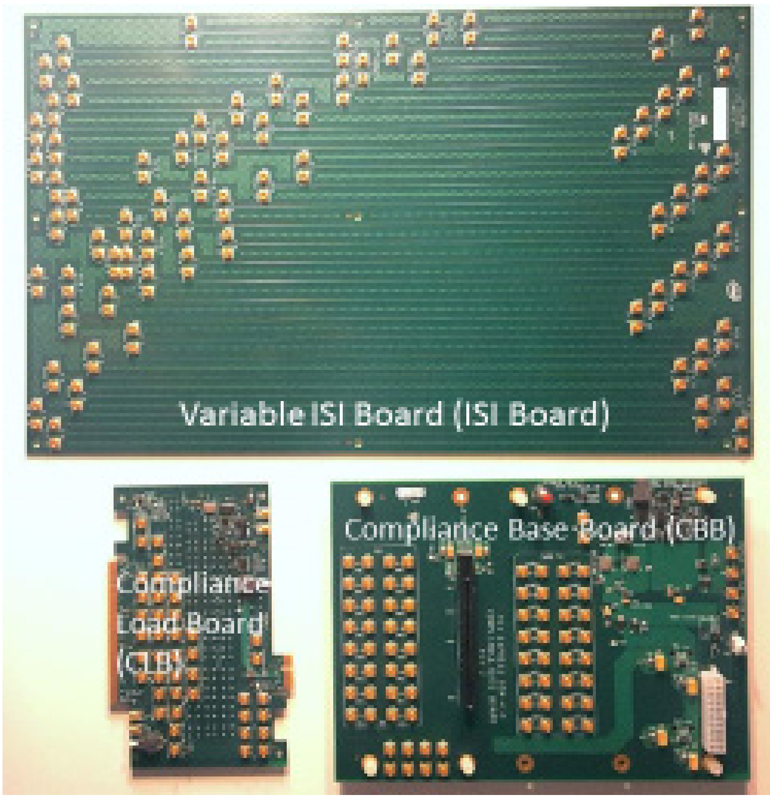

Figure 5. PCIe 4.0 Fixture Characterization Test Fixture Boards

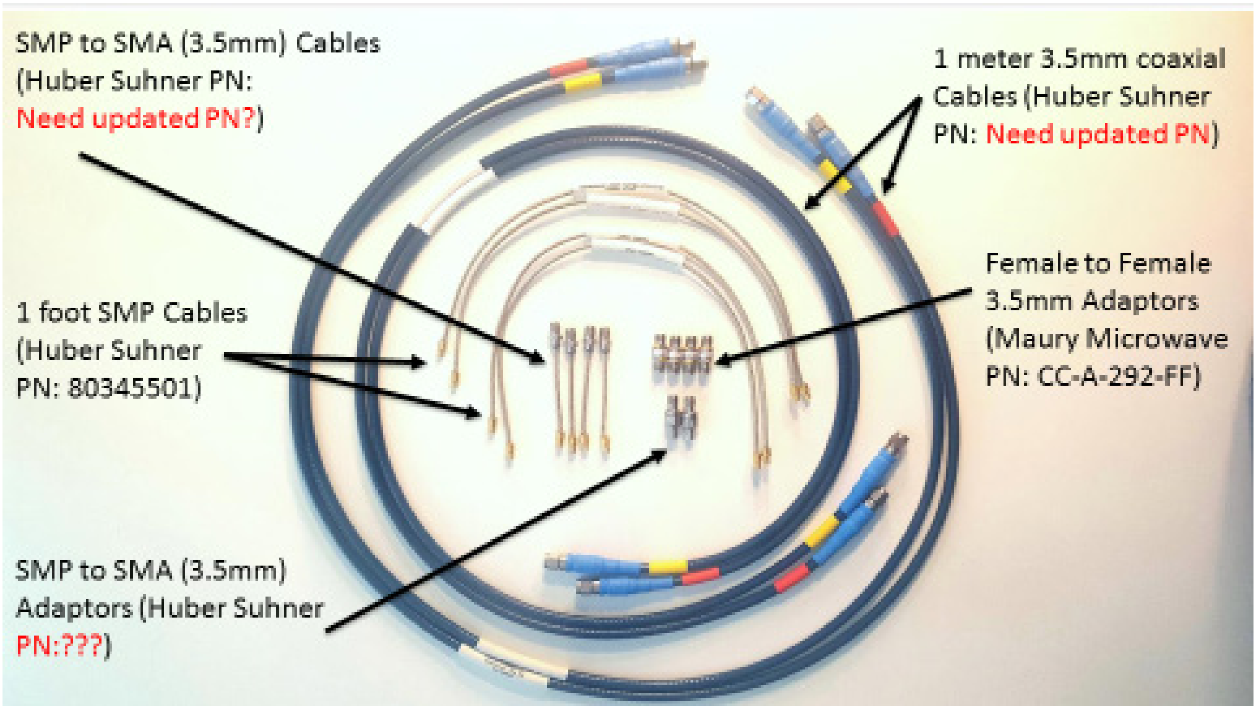

Figure 6. PCIe 4.0 Fixture Characterization Cables and Adapters

C.4 PCIe 4.0 Fixture Characterization Insertion Loss per Inch

- Determine loss per inch of PCBs
  The test fixture Insertion Loss (IL) per inch is necessary to estimate the differential trace IL of the CBB and CLB up to the CEM connector
- Short and long trace measurements (see Figure 7 and Figure 8)
  - SMP-to-SMA cables are included in these measurements
  - Measure IL of the short trace (J97/J99 to J96/J98) on the CBB
  - Measure IL of the long trace (J1/J74 to J2/J2/J73) on the CBB
  - The differential in length between the long trace and short trace is 10-inches.
  - IL/inch = (IL long trace – IL short trace)/10

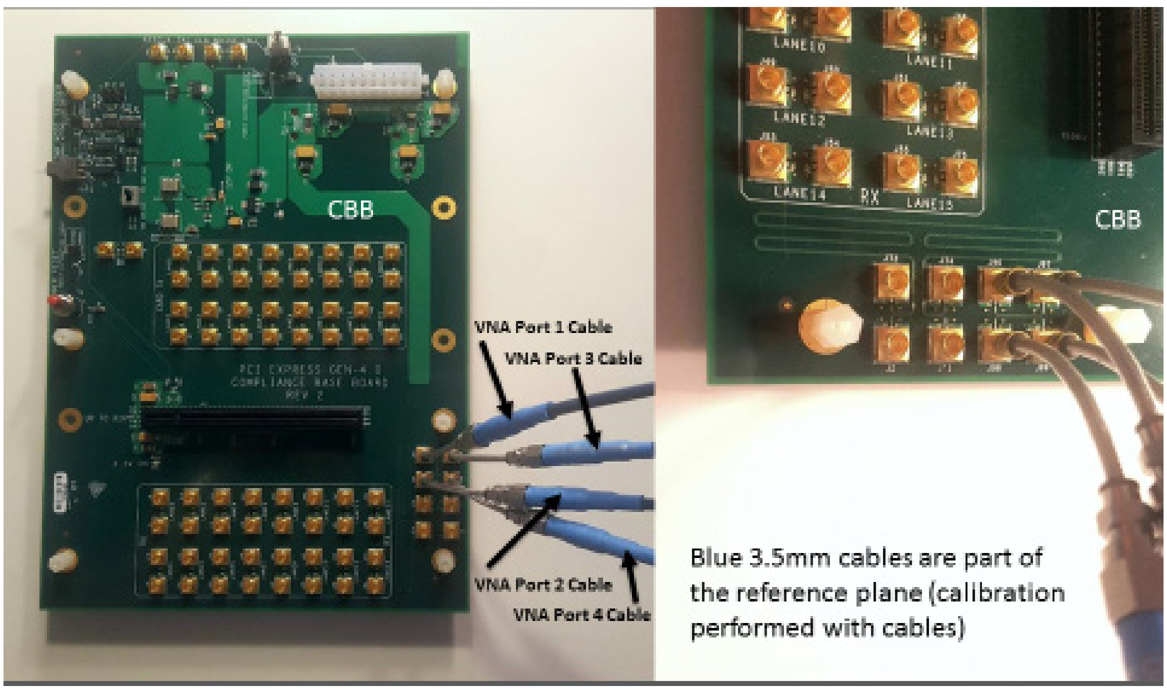

Figure 7. PCIe4.0 Fixture Characterization Insertion Loss per Inch (Short Trace)

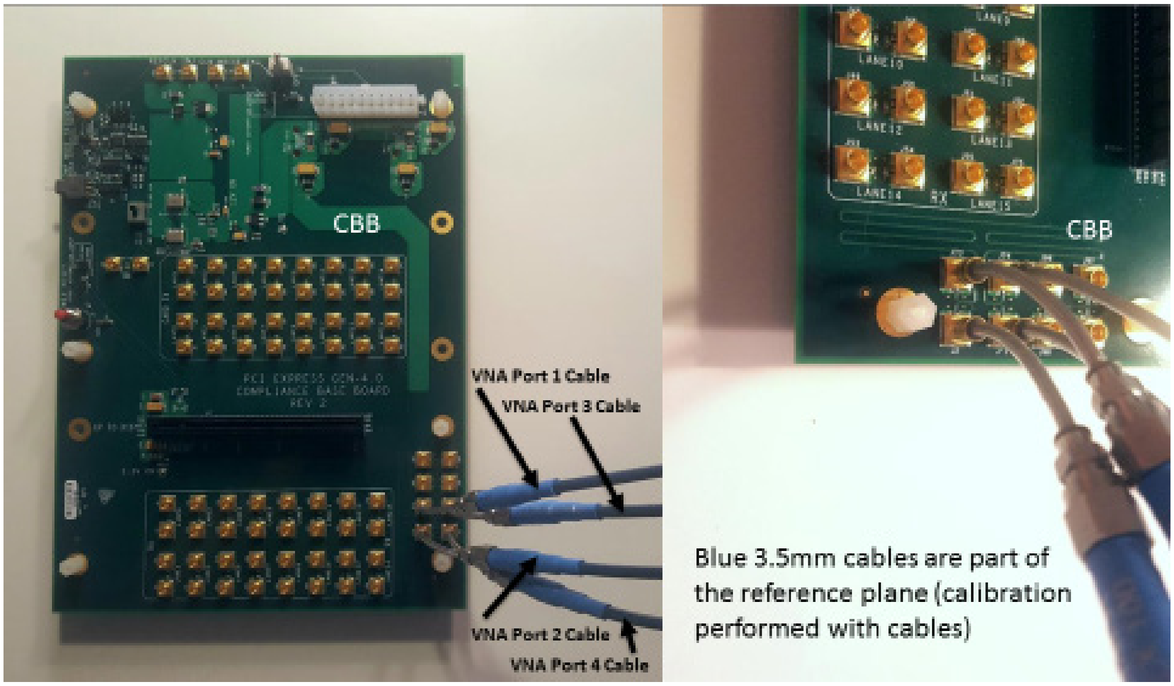

Figure 8. PCIe4.0 Fixture Characterization Insertion Loss per Inch (Long Trace)

C.5 PCIe 4.0 Fixture Characterization Coaxial Launch Loss

- Determine loss per SMB-to-SMA cable
  - SMP-to-SMA adapter IL must be comprehended for removal (see Figure 9).
  - If Huber Suhner adapters (PN 80350960) are used, an IL of 0.2225 dB is assumed
  - If different adapters are used, the IL must be measured.
    Possible measurement technique is:
    SMA-to-SMP adapter ←→ SMP-to-SMA cable
    If the IL of SMA-to-SMP adapter is known, this may be removed
- Coaxial launch loss
  - The coaxial launch loss IL is obtained from the long trace IL by removing the IL of the 10-inch trace and the two SMP-to-SMA cables
  - Coaxial launch IL = (IL long trace- (10-* IL/inch) – (2* IL SMP – SMA cable)) /2

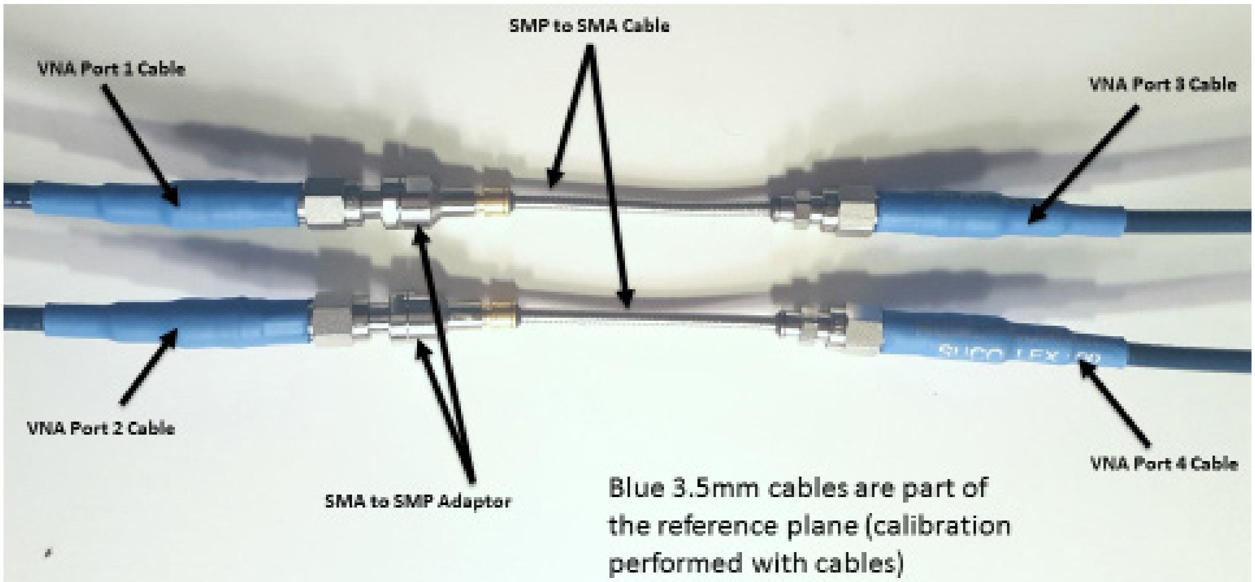

Figure 9. Characterize SMP-to-SMA Adapter

C.6 Measured CBB/CLB Loss

Determine the loss of CBB and CLB:

- Measure the IL of the CLB mated with the CBB establishes an easily measurable loss inclusive of the mated CEM connector (Figure 10).
- The mated CEM connector can then be obtained by removing the CLB RX Lane 0.
- Plug the CLB (x16) into the CBB and measure the IL

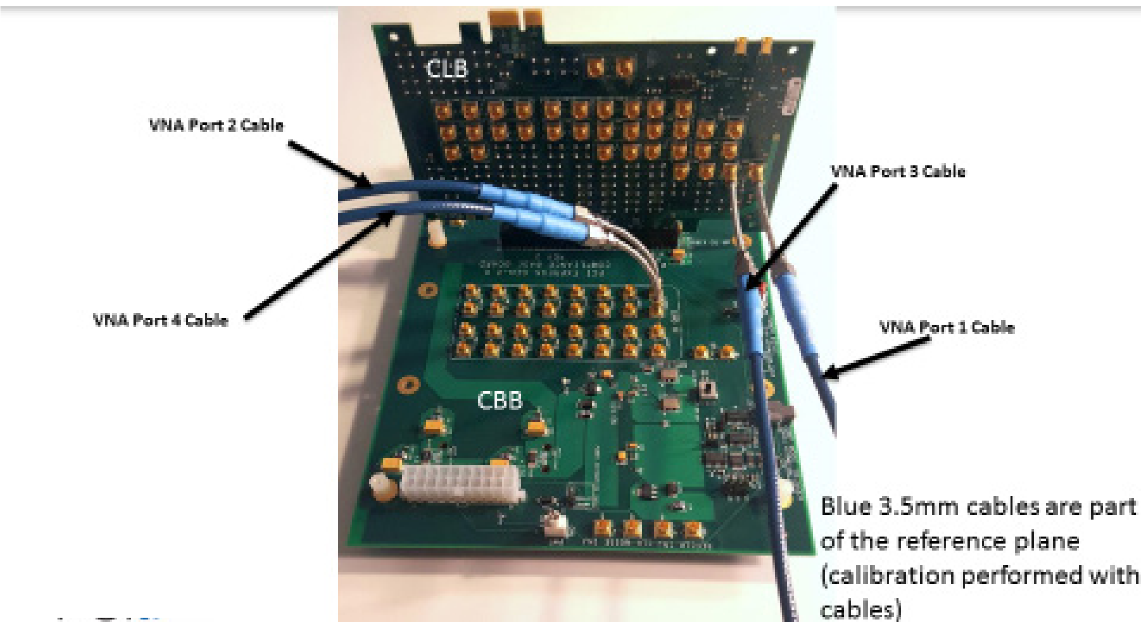

Figure 10. Measure CBB/CLB Loss (Image)

C.7 Mated CEM Connector Loss

Determine the loss of mated CEM connector:

- The mated CEM connector (edge fingers of CLB plugged into CEM connector) is needed to determine the IL on each side of the test fixture channels.
- The mated CEM connector loss is obtained by removing the IL of cables, coaxial launches, and traces from the CBB/CLB loss.
- Mated CEM IL = CBB/CLB IL = (2* Coaxial Launch IL)
  - CBB Trace Length = 3-iinches
  - CLB Trace Length = 4-inches

  Typical mated CEM IL is around 1.2 dB

C.8 Determine Loss Split for CBB and CLB

- Determine loss of CBB (including mated CEM connector loss)
  - The mated CEM connector IL is part of a system IL budget and is included on the CBB side.
  - CBB IL = Mated CEM IL + (IL/Inch * CBB Trace Length) +2* Coaxial Launch IL) CBB Trace Length = 3-inches
- Determine loss of CBL (excluding mated CEM connector loss)
  CLB Loss = (IL/Inch + CLB Trace Length) + (2 * Coaxial Launch IL) CLB Trace Length = 4-inches.

C.9 Finding Correct Variable ISI Pairs

- Target loss for each test configuration are determined based on the CBB and CLB loss
- VNA measurements are taken to find the variable ISS Pir matching the target loss
  - There are two measurement setups:
    - Variable ISI Cables (TX test and DUT side during RX calibration)
    - Full calibration channel (RX calibration – 27/28/30 dB channels)
      All cables included.
  - If the measurement is less than the target loss, the variable ISI pair is increased.
  - If the measurement is more than the target loss, the variable ISI pair is decreased.
  - Nominally, there should be 0,5 dB steps between ISI pairs.

C.10 Target Loss Values – System RX

Determine target loss for system RX and find correct variable ISI pair.

- Variable ISI with cables (ISI board, SMP cable, and SMA cable), see Figure 11.
- System RX calibration CBB side (20 dB fixed)
  - Target loss – 20 dB – 5 dB (package embedded) -CBB loss
  - Measure setup:
    SMP cable ⍰⍰ Variable ISI Pair X ⍰⍰ SMA cable.
  - Full calibration Channel (see Figure 12)
    - System RX calibration CLB ISI (Low – 27 dB)
      Target loss = 27 dB – 5 dB (package embedded)
    - System RX calibration CLB ISI (Nominal – 20 dB)
      Target loss = 28 dB – 5 dB (package embedded)
    - System RX calibration CLB ISI (High – 30 dB)
      Target loss = 30 dB – 5 dB (package embedded)

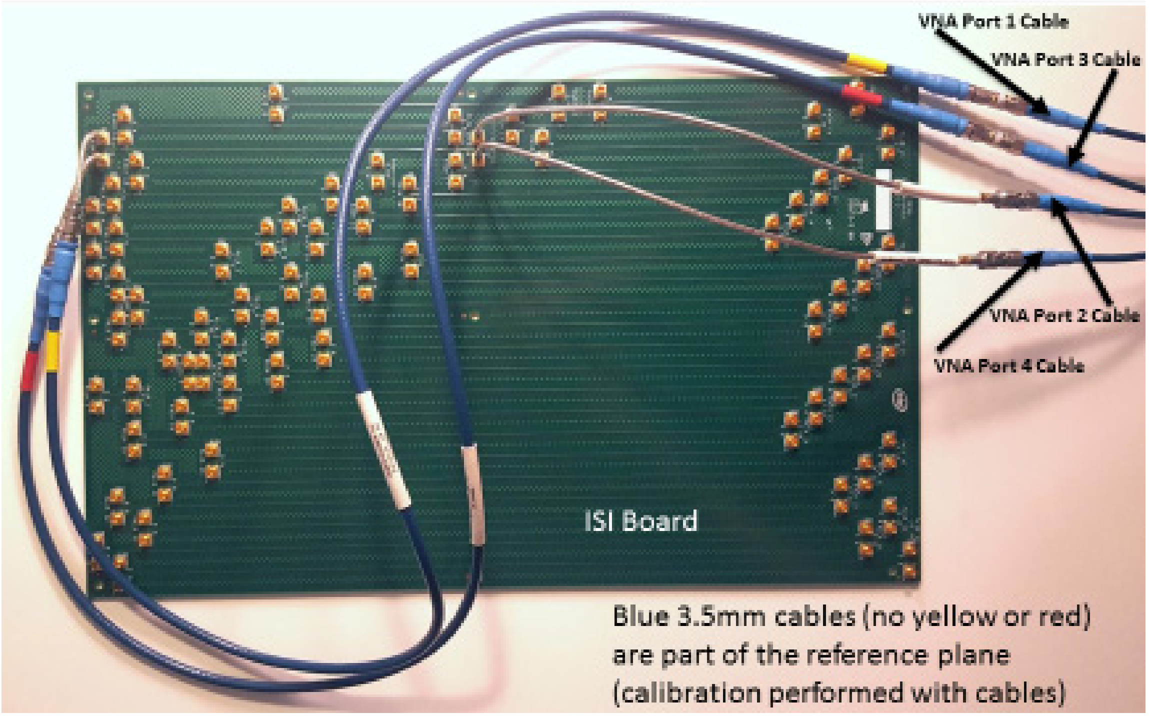

Figure 11. System RX CAL (Variable with Cables)

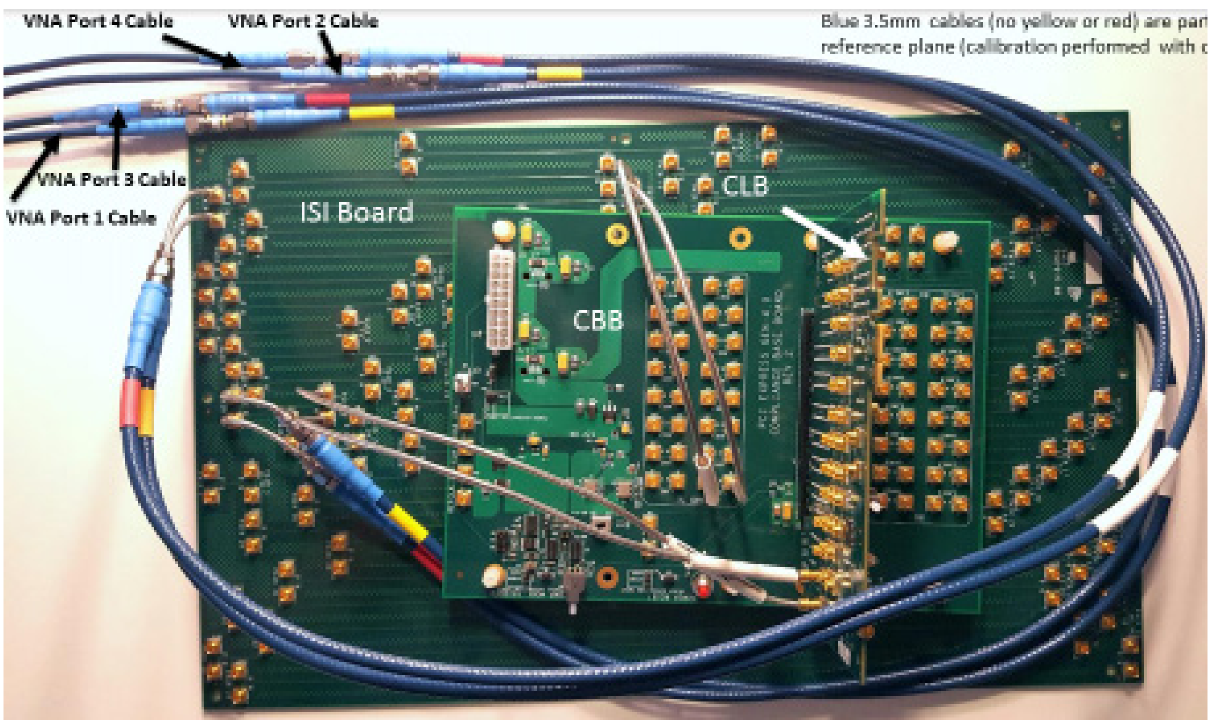

Figure 12. System RX CAL (Full with Cables)

C.11 Target Loss Values – Add-in Card RX

Determine target loss for system Add-in Card RX and find correct variable ISI pair.

- ❑ Variable ISI with cables (ISI board, SMP cable, and SMA cable), see Figure 13.
- ❑ Add-in Card calibration CLB side (8 dB fixed)
  - Target loss – 8 dB – 3 dB (package embedded) -CLB loss
  - Measure setup:
    SMP cable ←→ Variable ISI Pair X ←→ SMA cable.
- ❑ Full calibration Channel (see Figure 14)
  - Add-in Card RX calibration CBB ISI (Low – 27 dB)
    Target loss = 27 dB – 3 dB (package embedded)
  - Add-in Card RX calibration CBB ISI (Nominal – 28 dB)
    Target loss = 28 dB – 5 dB (package embedded)
  - Add-in Card RX calibration CBB ISI (High – 30 dB)
    Target loss = 30 dB – 3 dB (package embedded

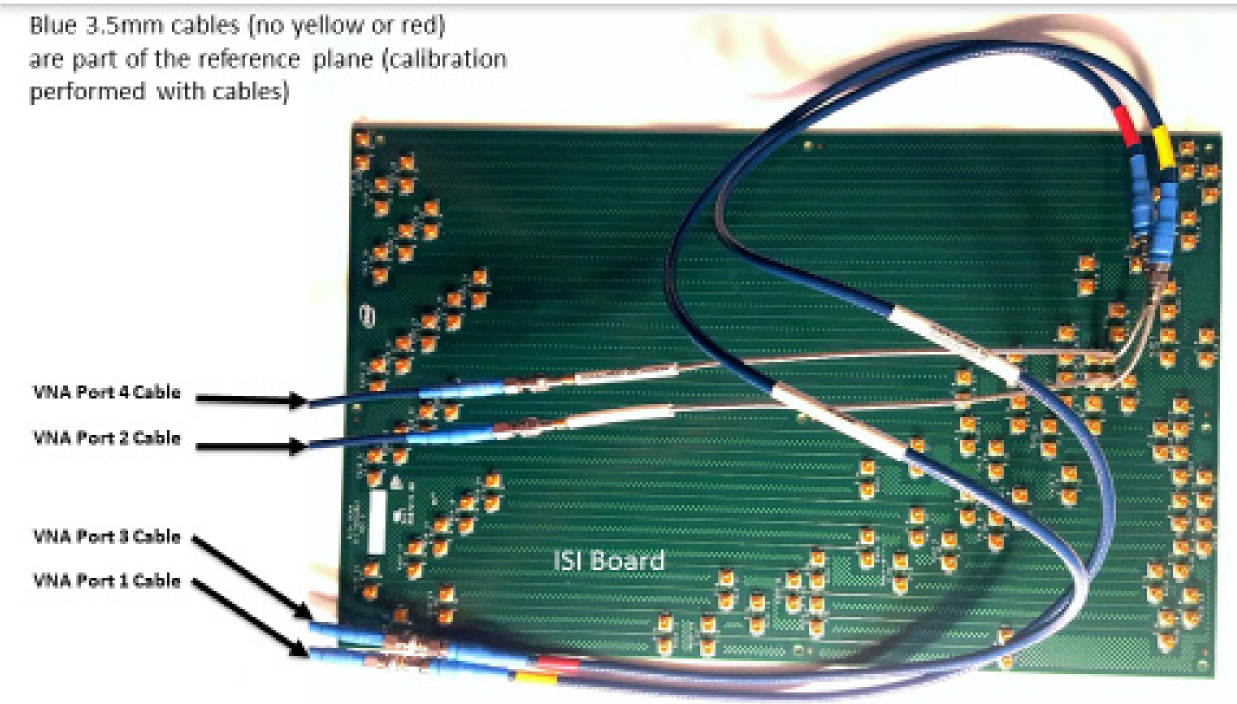

Figure 13. AIC RX CAL (Variable ISI with Cables)

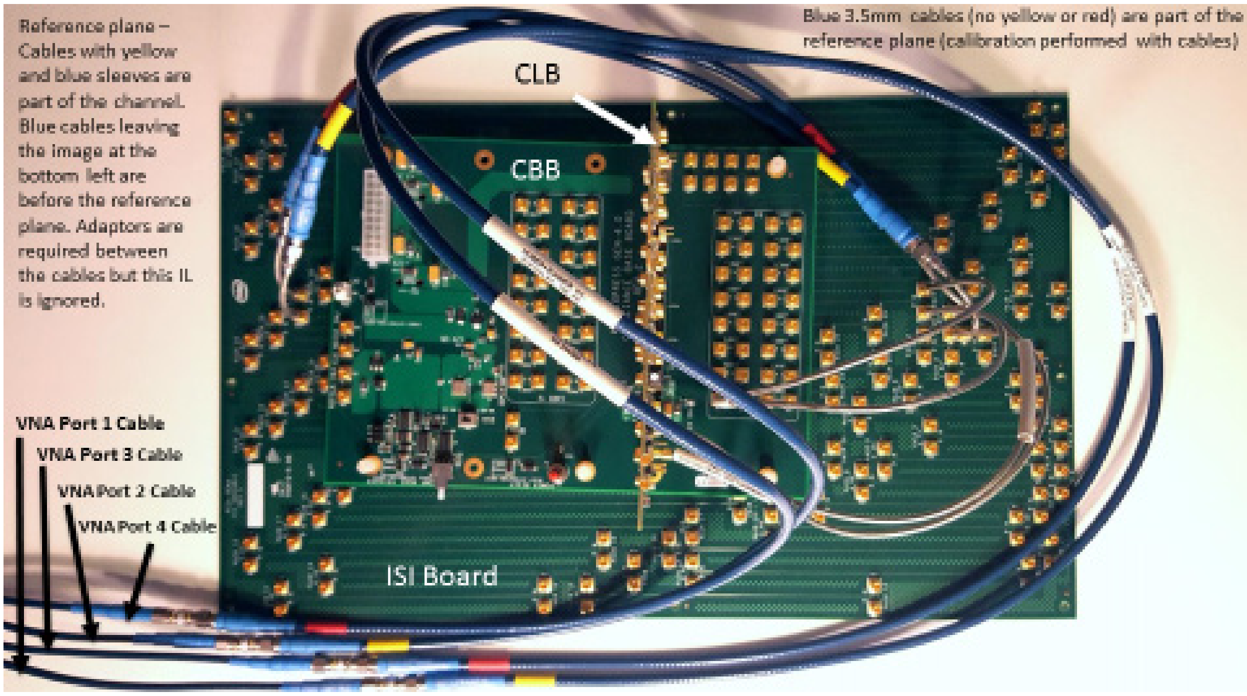

Figure 14. AIC RX CAL (Full Calibration Channel)

C.12 Target Loss Values – TX Signal Quality

Determine target loss for Add-in Card RX and find correct variable ISI pair.

- ❑ Variable ISI with cables (ISI board, SMP cable, and SMA cable), see Figure 15.
  - System TX signal quality test
    Target loss = 8 dB – 3 dB (package embedded – CLB Loss
- ❑ Add-in Card calibration CLB side (8 dB fixed), see Figure 16
  - Target loss – 8 dB – 3 dB (package embedded) -CLB loss
    Measure setup:
  - SMP cable ←→Variable ISI Pair X ←→ SMA cable.
  - Add-in Card TX signal quality
    Target loss = 20 dB (package embedded) – CBB loss

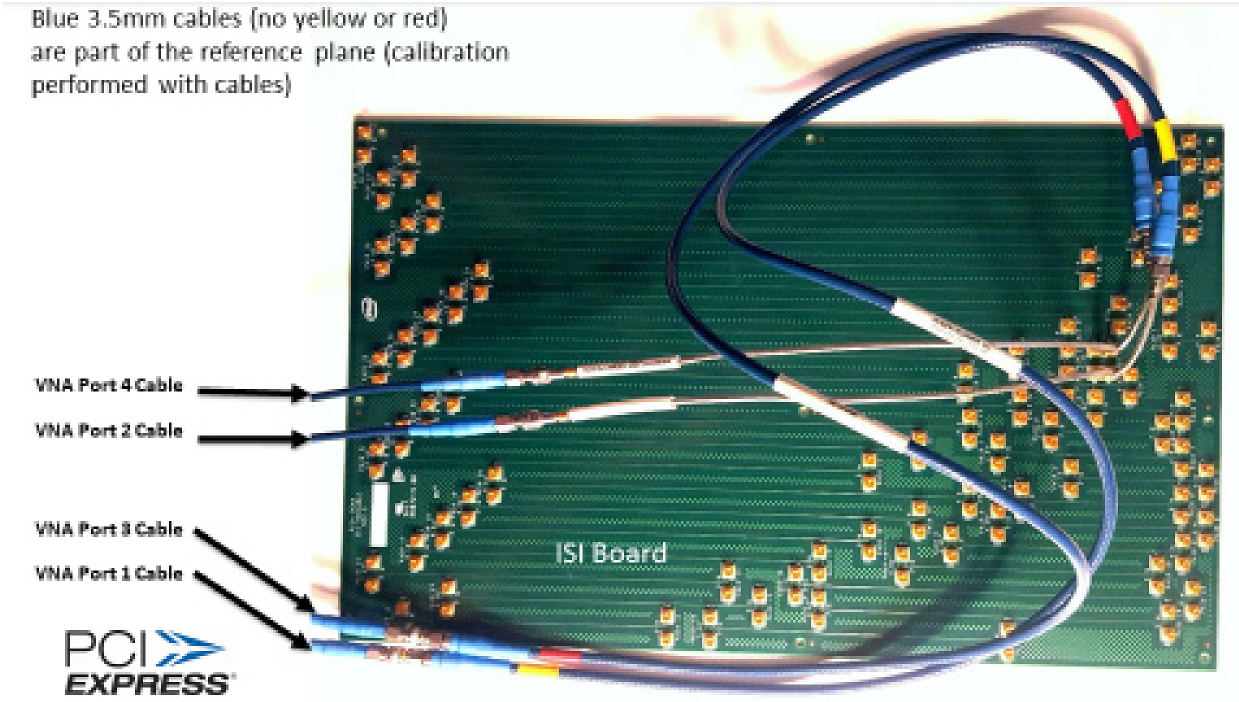

Figure 15. AIC TX (Variable calibration with cables)

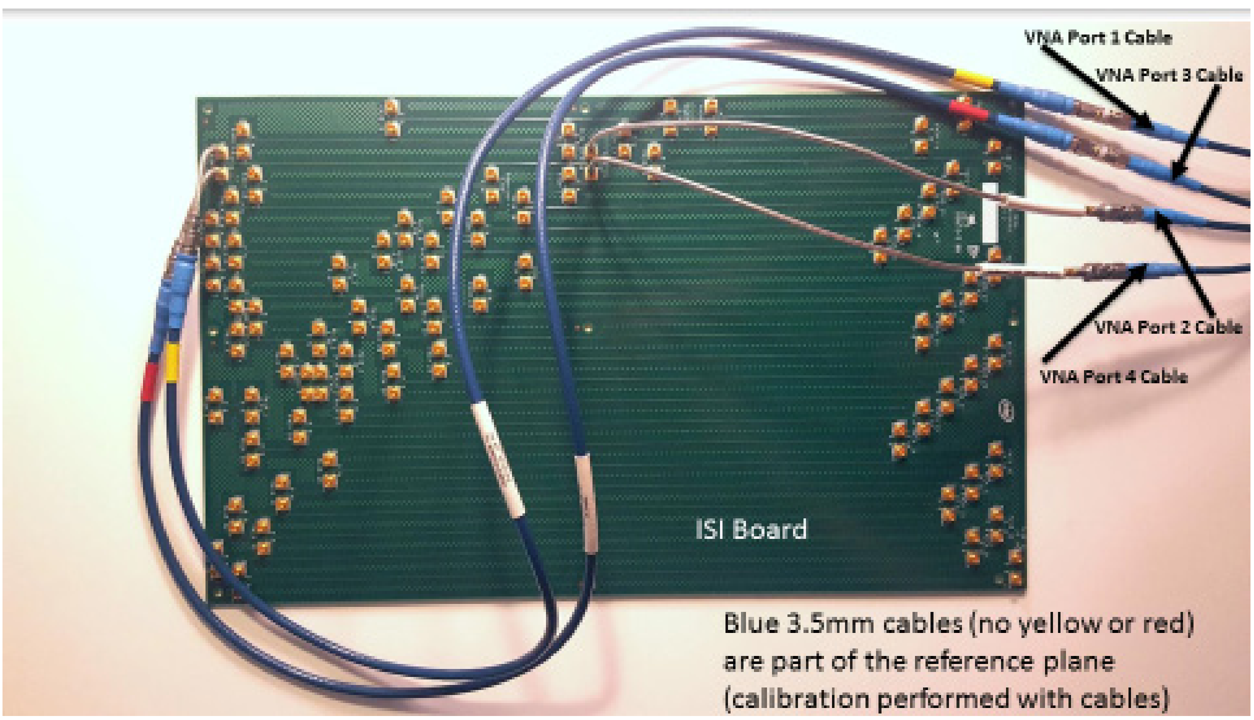

Figure 16. System TX = (Variable ISI with Cables)

C.13 Spread Sheet for Fixture Calibration

Refer to the attached spreadsheet for fixture calibration.

Click on the Attachment icon in the left column on this PDF to access the Excel™ spreadsheet.

D

Appendix D. Alternate Method of System TX Signal Quality Test at 16GT/s

An alternate method of performing 16GT/s System Signal Quality test is provided in this note. The data and 100 MHz reference clock can be captured and post-processed separately. The data will be processed with SigTest using the 16GT/s Add-in Card Signal Quality template file (PCIe_4_16G_CEM.dat). The pass/fail limits for Eye Width at 1E-12 and Eye Height at 1E-12 will remain unchanged for 16 GT/s System Signal Quality Test. The reference clock will be post-processed with a separate clock tool to ensure the Random Jitter is less than 0.7 ps RMS as defined in the *PCI Express Base Specification*.

E

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